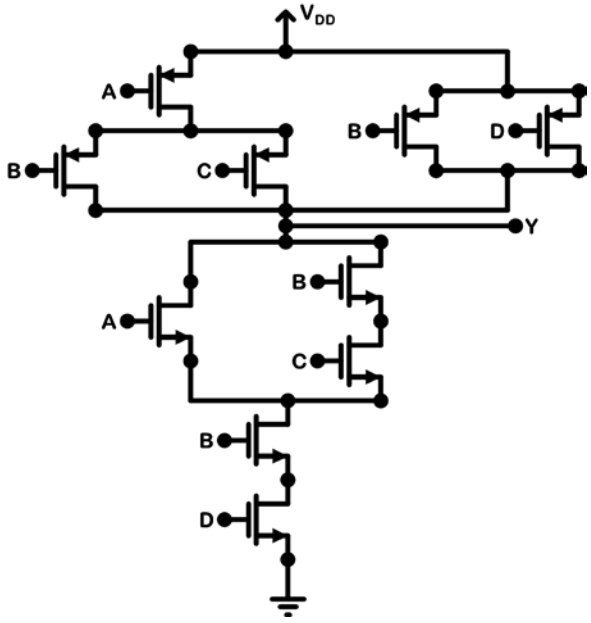
EECS312-HW10: CMOS Logic Design

1. **For the following logic functions:**
   a. **Design the PUN and PDN.**
   b. **Identify the input combinations that the PUN will be conducting and for each combination determine the PUN resistance, r_{PUN}, in terms of r_{SDP} of a single PMOS component.**
   c. **Identify the input combinations that the PDN will be conducting and for each combination determine the PDN resistance, r_{PDN}, in terms of r_{DSN} of a single NMOS component.**
   d. **Using $k_n=k_p=4mA/V^2$, $V_{tn}=|V_{tp}|=1V$, and $V_{DD}=3V$, determine r_{DSN} and r_{SDP}.**
   e. **For an output capacitance of C=50pF, determine the maximum value of T_{PLH} and T_{PHL}.**

$$Y = \overline{A} \cdot \overline{B \cdot C} + \overline{D \cdot B}$$
$$Y = \overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{C} + \overline{D} + \overline{B}$$

$r = r_{DSN} = r_{SDP} = 1/(.004(3-0.8)) = 114\Omega$

ABCD	r_{PUN}	r_{PDN}
0000	(r+r/2)||(r/2)	open
0001	(r+r/2)||(r)	open
0010	(2r)||(r/2)	open
0011	(2r)||(r)	open
0100	(2r)||(r)	open
0101	(r)	open
0110	(r)	open
0111	open	(4r)
1000	(r/2)	open
1001	(r)	open
1010	(2r)	open
1011	(r)	open
1100	(r)	open
1101	open	(3r)
1110	(r)	open
1111	open	(2r)+(r||2r)

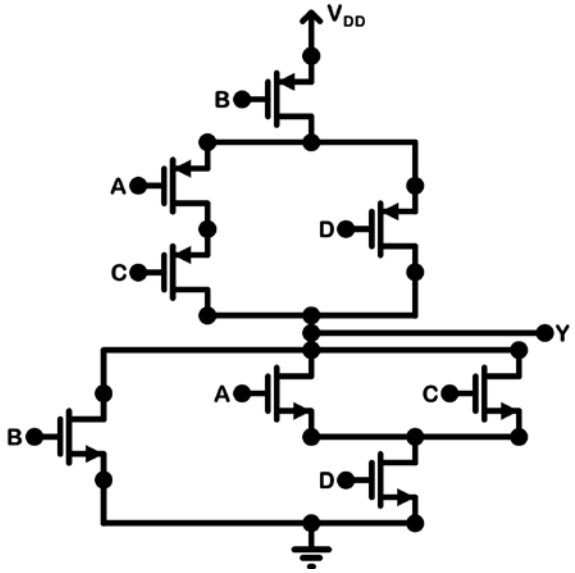


$r_{PUN\_MAX} = 2r = 228\Omega$
$r_{PDN\_MAX} = 4r = 456\Omega$
$\tau_{PLH} = 50x10^{-12} \cdot 228 \cdot \ln(2) = 8ns$
$\tau_{PHL} = 50x10^{-12} \cdot 456 \cdot \ln(2) = 16ns$

Sizes of PMOS: $(W/L)_{A,B1,C} = 2p$
$(W/L)_{B2,D} = p$
Sizes of NMOS: $(W/L)_{B1,B2,C,D} = 4n$
$(W/L)_{A} = 2n$
Could be simplified using the equation: $Y = \overline{A} \cdot \overline{C} + \overline{D} + \overline{B}$

$$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{D + B}$$
$$Y = \overline{B} \cdot \left(\overline{A} \cdot \overline{C} + \overline{D}\right)$$

ABCD	r_{PUN}	r_{PDN}
0000	r+(2r||r)	open
0001	3r	open
0010	2r	open
0011	open	2r
0100	open	r
0101	open	r
0110	open	r
0111	open	r||2r
1000	2r	open
1001	open	2r
1010	2r	open
1011	open	r+r/2
1100	open	r
1101	open	r||2r
1110	open	r
1111	open	r||(r+r/2)



r_{PUN_MAX} = 3r = 342Ω
r_{PDN_MAX} = 2r = 228Ω
τ_{PHL} = $50x10^{-12} \cdot 228 \cdot \ln(2)$ = 8ns
τ_{PLH} = $50x10^{-12} \cdot 342 \cdot \ln(2)$ = 12ns

Sizes of PMOS: $(W/L)_{A,B,C}$ = 3p
$(W/L)_{D}$ = 3p/2
Sizes of NMOS: $(W/L)_{A,C,D}$ = 2n
$(W/L)_{B}$ = n

2. A one-bit full adder with carry in/out has three inputs and two outputs.

Inputs:

- A: First coefficient.
- B: Second coefficient.
- C_{IN}: Carry input from previous stage.

Outputs

- S: Sum.
- C_{OUT}: Carry output.

a. Determine the logic functions for S and C_{OUT} in terms of A, B, and C_{IN}. Remember, for CMOS design you can only use ANDs, ORs, and NOTs in your logic functions.

Truth Table

A	B	C_{IN}	S	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

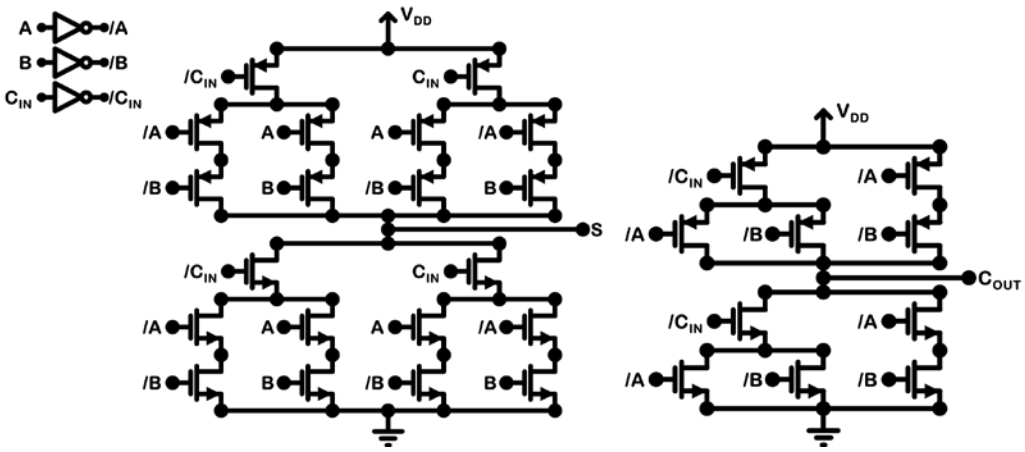
$S = /A \cdot /B \cdot C_{IN} + /A \cdot B \cdot /C_{IN} + A \cdot /B \cdot /C_{IN} + A \cdot B \cdot C_{IN}$
$S = /A \cdot /B \cdot C_{IN} + A \cdot B \cdot C_{IN} + /A \cdot B \cdot /C_{IN} + A \cdot /B \cdot /C_{IN}$
$S = C_{IN} \cdot (/A \cdot /B + A \cdot B) + /C_{IN} \cdot (/A \cdot B + A \cdot /B)$

$/S = /A \cdot /B \cdot /C_{IN} + /A \cdot B \cdot C_{IN} + A \cdot /B \cdot C_{IN} + A \cdot B \cdot /C_{IN}$
$/S = = C_{IN} \cdot (A \cdot /B + A \cdot /B) + /C_{IN} \cdot (A \cdot B + /A \cdot /B)$

$C_{OUT} = /A \cdot B \cdot C_{IN} + A \cdot /B \cdot C_{IN} + A \cdot B \cdot /C_{IN} + A \cdot B \cdot C_{IN}$
$C_{OUT} = /A \cdot B \cdot C_{IN} + A \cdot /B \cdot C_{IN} + A \cdot B \cdot /C_{IN} + A \cdot B \cdot C_{IN} + A \cdot B \cdot C_{IN} + A \cdot B \cdot C_{IN}$
$C_{OUT} = (/A \cdot B \cdot C_{IN} + A \cdot B \cdot C_{IN}) + (A \cdot /B \cdot C_{IN} + A \cdot B \cdot C_{IN}) + (A \cdot B \cdot /C_{IN} + A \cdot B \cdot C_{IN})$
$C_{OUT} = (B \cdot C_{IN}) + (A \cdot C_{IN}) + (A \cdot B)$
$C_{OUT} = C_{IN} \cdot (A+B) + A \cdot B$

$/C_{OUT} = /A \cdot /B \cdot /C_{IN} + /A \cdot /B \cdot C_{IN} + /A \cdot B \cdot /C_{IN} + A \cdot /B \cdot /C_{IN}$
$/C_{OUT} = (/A \cdot /B \cdot /C_{IN} + /A \cdot /B \cdot C_{IN}) + (/A \cdot /B \cdot /C_{IN} + /A \cdot B \cdot /C_{IN}) + (A \cdot /B \cdot /C_{IN} + /A \cdot /B \cdot /C_{IN})$
$/C_{OUT} = (/A \cdot /B) + (/A \cdot /C_{IN}) + (/B \cdot /C_{IN})$
$/C_{OUT} = /A \cdot /B + /C_{IN} \cdot (/A + /B)$

b. Implement the each logic function in CMOS.



c. Determine how many PMOS and NMOS transistors are required.

Inverters: 3PMOS, 3NMOS
Sum: 10PMOS, 10NMOS
Carry: 5PMOS, 5NMOS
Total: 18PMOS, 18NMOS

d. Using $k_n=k_p=20mA/V^2$, $V_{tn}=|V_{tp}|=0.8V$, and $V_{DD}=2.5V$, determine r_{DSN}, r_{SDP}.

$r_{DSN} = r_{SDP} = 1/(.02(2.5-.8)) = 30\Omega$

e. For an output capacitance of C=40pF, determine the maximum propagation delay for carry output, C_{OUT}, based on the maximum PUN or PDN resistance.

$\tau_{PHL} = \tau_{PLH} = 40x10^{-12}\cdot(2\cdot30)\cdot\ln(2) = 1.7ns$

f. What would the maximum net delay be for an 8-bit inverter and resulting maximum clock rate?

delay = $8\cdot\tau_P$ = 13ns
f_{MAX} = 1/13ns = 75MHz

note: If you need to use an inverter to a satisfy the function syntax for the PUN or PDN, just use the inverter symbol in part b and assume (1 PMOS and 1 NMOS) per inverter in part c, and assume the inverter has zero propagation delay for parts e & f.