EECS312-HW10: CMOS Logic Design Due 04/10/26

1. For the following logic functions:
   a. Design the PUN and PDN.
   b. Identify the input combinations that the PUN will be conducting and for each combination determine the PUN resistance, r_{PUN}, in terms of r_{SDP} of a single PMOS component.
   c. Identify the input combinations that the PDN will be conducting and for each combination determine the PDN resistance, r_{PDN}, in terms of r_{DSN} of a single NMOS component.
   d. Using $k_n=k_p=5mA/V^2$, $V_{tn}=|V_{tp}|=1V$, and $V_{DD}=3V$, determine r_{DSN} and r_{SDP}.

$$Y = \overline{A} \cdot \overline{B \cdot C} + \overline{D} \cdot \overline{B}$$

$$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{D + B}$$

2. A one-bit full adder with carry in/out has three inputs and two outputs.

   Inputs:
   - A: First coefficient.
   - B: Second coefficient.
   - C_{IN}: Carry input from previous stage.

   Outputs
   - S: Sum.
   - C_{OUT}: Carry output.

   a. Determine the logic functions for S and C_O in terms of A, B, and C_I. Remember, for CMOS design you can only use ANDs, ORs, and NOTs in your logic functions.
   b. Implement the each logic function in CMOS.
   c. Determine how many PMOS and NMOS transistors are required.
   d. Using $k_n=k_p=20mA/V^2$, $V_{tn}=|V_{tp}|=0.8V$, and $V_{DD}=2.5V$, determine r_{DSN}, r_{SDP}.

   note: If you need to use an inverter to a satisfy the function syntax for the PUN or PDN, just use the inverter symbol in part b and assume (1 PMOS and 1 NMOS) per inverter in part c.