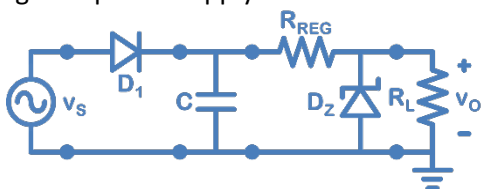
EECS312-HW6: Designing a 9V power supply based on the circuit below.



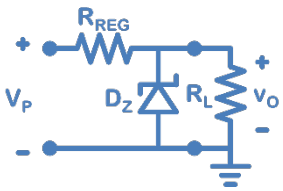
A transformer has been used to step down the 120Vrms outlet voltage to 12Vpeak:

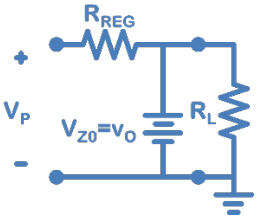
$$v_S(t) = 12\cdot\cos(2\pi 60t)$$

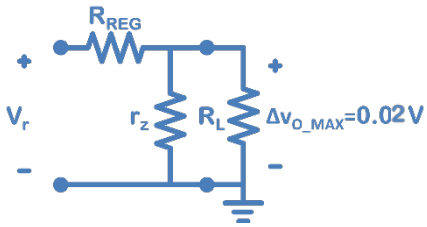
The rectifier diode, D_1, is modeled as a 0.7V CVD and the Zener diode, D_Z, has parameters of r_z=8Ω and V_{Z0} = 8.8V. The load is modeled using resistance, R_L=160Ω. What is the peak voltage at the output of the rectifier (D1:cathode, Top of the Capacitor) ?

V_P = 12-0.7=11.3[V]

The circuit below (**left circuit**) will be used to find the value for R_{REG}, assuming the input voltage has a constant value of V_P. Replace the Zener diode with a 9V CVD model (5V battery – **center circuit**) and find the maximum value of R_{REG} that ensures the ideal diode remains forward biased (conducting). Choose an actual value that is 70% the maximum to include some error margin.







R_{REGMAX} = (11.3-9)/R_{REG}>9/160 R_{REG}<160·(11.3-9)/9=40.89[Ω]

R_{REG} = 0.7·40.89=28.62[Ω]

Find the line regulation ($\Delta v_O/V_r$ – **right circuit**) using R_{REG}, r_z, and R_L.

Line Reg = 160||8/(28.62+160||8) = 0.21[V/V]

If we want a maximum ripple at the output, Δv_O, to be 0.02V, what is the allowable ripple, V_r, at the input of the regulator (based on the Line Reg)?

V_r = 0.21*V_r=.02 V_r=.02/0.21=0.095[V]

Find the effective resistance, R_C, that would be in parallel with the filter capacitor. Also, find the minimum capacitance to meet the ripple voltage, V_r.

R_C = R_C=11.3*28.62/(11.3-9) = 140.6

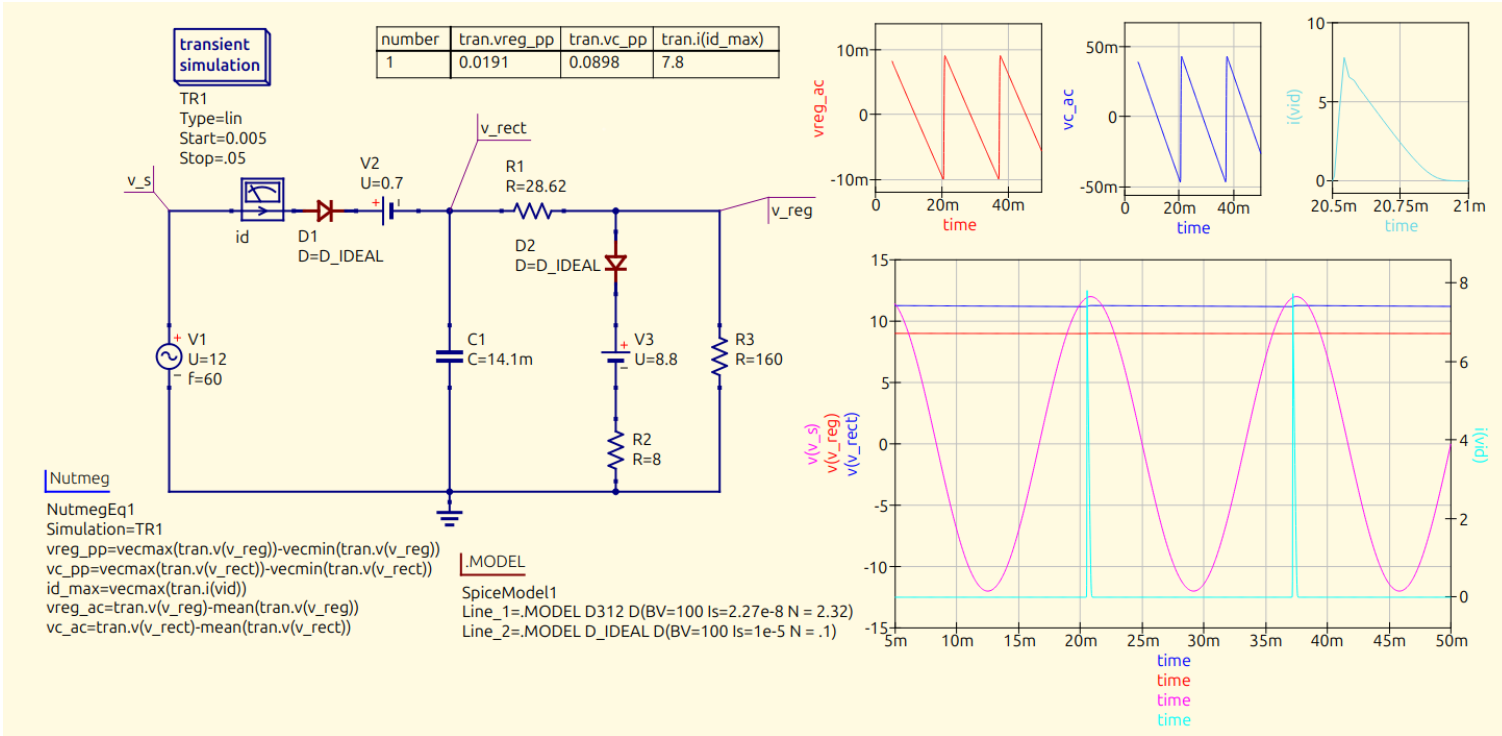
C = C=11.3/(60*140.6*.095) = 14.1mF

Find the duration the rectifier diode is conducting and the maximum current through the diode.

Δt = 0.344ms

I_{DMAX} = 11.3/140.6*2*(1+1/(60*.000344) = 7.95A

Run a simulation using your circuit simulator to generate plots of $v_S(t)$, $v_C(t)$, $v_O(t)$, and $i_D(t)$. Estimate values for V_r, Δv_O, Δt, and I_{DMAX} from the plots.


transient simulation
TR1
Type=lin
Start=0.005
Stop=.05
number | tran.vreg_pp | tran.vc_pp | tran.i(id_max)
1 | 0.0191 | 0.0898 | 7.8
v_s
id
V2
U=0.7
D1
D=D_IDEAL
v_rect
R1
R=28.62
D2
D=D_IDEAL
v_reg
V1
U=12
f=60
C1
C=14.1m
V3
U=8.8
R3
R=160
R2
R=8
Nutmeg
NutmegEq1
Simulation=TR1
vreg_pp=vecmax(tran.v(v_reg))-vecmin(tran.v(v_reg))
vc_pp=vecmax(tran.v(v_rect))-vecmin(tran.v(v_rect))
id_max=vecmax(tran.i(vid))
vreg_ac=tran.v(v_reg)-mean(tran.v(v_reg))
vc_ac=tran.v(v_rect)-mean(tran.v(v_rect))
.MODEL
SpiceModel1
Line_1=.MODEL D312 D(BV=100 Is=2.27e-8 N = 2.32)
Line_2=.MODEL D_IDEAL D(BV=100 Is=1e-5 N = .1)
vreg_ac
vc_ac
i(vid)
time
v(v_s)
v(v_reg)
v(v_rect)
i(vid)