EECS 312 – Electronic Circuits I – 3 Credit Hours
Spring 2025 – 1136 Learned – 12:00-12:50 pm

Instructor: Carl Leuschen
Office: 3014 Eaton Hall & 311 Nichols Hall

Office Hours: 11:00-11:50 am MWF by appointment.
if these times don't work, email me.

E-mail: leuschen@ku.edu

Text: Microelectronic Circuits, Adel S. Sedra and Kenneth C. Smith, 7th Edition, 2015

Website: http://people.eecs.ku.edu/~leuschen/

Grading Components:

Homework	15%
Quizzes	30%
Exams (2)	30%
Final	25%

Scale:

100-93	A
93-90	A-
90-87	B+
87-83	B
83-80	B-
80-77	C+
77-73	C
73-70	C-
70-67	D+
67-63	D
63-60	D-
60-0	F

Homework: Homework will be assigned in class and/or on the class website. It is your responsibility to check the website for updates to schedules and due dates. Late assignments will NOT be accepted for full credit. Copying others work or providing work for others to copy is not acceptable (see Ethics Policy). Homework assignments will be submitted before class on the due date (stapled, folded lengthwise, no work on the outside except the following info shown below). Assignments submitted during class will lose 5%. Late assignments will lose **at least 10% per day** (for up to 3 days **at the discretion of the instructor**). Clearly circle each answer and make sure your work is legible (If I can't read it, it won't get credit). HW submissions should be folded lengthwise, stapled, and the only thing on the outside should be in the same order (Failure to do so can result in 10% deduction):

NAME (Last, First)	Leuschen, Carl
KUID	123456
HW#	HW#00
Date	1/27/25

Quizzes: Short quizzes will be administered throughout the semester. They will not always be announced ahead of time.

Exams & Final: There will be two exams during the semester with tentative dates identified in the course schedule. The final will be comprehensive of all material covered during the semester. Use of an approved calculator and/or cheat sheet will be decided prior to the exams.

Policies:

Ethics Policy: Academic misconduct (cheating, giving help, copying, representing others work as your own …) will not be tolerated. It will result in a failing grade, be reported to the Department/Dean, and may result in further disciplinary action by the University. For details see the Academic Misconduct section of the Timetable.

Participation: Attendance and participation are expected in class – no cell phone usage during lectures, and no third party note taking.

Handguns: Individuals who choose to carry concealed handguns are solely responsible to do so in a safe and secure manner in ***strict conformity with state and federal laws and KU weapons policy***. Information at http://concealedcarry.ku.edu/information.

Illness: The knowledge and skills you will gain in this course highly depend on your participation in class activities. Because of that, I expect you to attend all class sessions unless you are ill or have a valid reason for missing. **If you are unable to attend class, contact me by email in advance of the absence (not afterward).**

Accommodations:

The Student Access Center coordinates academic accommodations and services for all eligible KU students with disabilities. If you have a disability for which you wish to request accommodations and have not contacted the Student Access Center, please do so as soon as possible. The center is located in 22 Strong Hall and can be reached at 785-864-4064. Information about its services can be found at www.access.ku.edu. Please contact me privately in regard to your needs in this course

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Description: Introduction to diodes, MOSFET's and their use in electronics, especially digital circuits.

Outcomes: Students should be able to:

1. Understand and identify all technical names, bias modes, device equations, and circuit approximations for diodes.
2. Understand and identify all technical aspects of MOSFET transistors, including terminal names, bias modes, and device equations.
3. Understand the operation of CMOS digital logic circuits, in order to determine or verify characteristic quantities such as logic levels, noise margins, switching times, and power dissipation.

Key Topics:

1. Diode terminal characteristics and forward biasing.
2. Reverse biasing, Zener diode, and rectifier circuits.
3. Diode-based limiting circuits, special diodes.
4. MOSFET structure, current-voltage characteristics.
5. MOSFET circuit DC analysis and amplifier design.
6. MOSFET circuit small-signal analysis, MOSFET Body effect.
7. Digital-logic inverters.
8. CMOS inverter and dynamic operation.
9. CMOS logical-gate circuits, Latches, flip-flops.
10. Semiconductor memory architecture and RAM.

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	#	Day	Date	Topic	Reading Due.
Intro		Mon	(01/20)	MLK Holiday	
	1	Wed	(01/22)	Intro (syllabus & Schedule), Circuits Review	
	2	Fri	(01/24)	Review, I-V Relationships, Linearity	
Diodes	3	Mon	(01/27)	The Diode (Ideal), Applications: Digital Logic	4, 4.1, Ideal Diode Notes
	4	Wed	(01/29)	The Junction Diode	4.2, Junction Diode Notes
	5	Fri	(01/31)	Modeling the Forward Bias Region	4.3
	6	Mon	(02/03)	Small Signal Model Analysis	Diode Small Signal Notes
	7	Wed	(02/05)	The Diode Small Signal Model, Apps: Voltage Regulator	
	8	Fri	(02/07)	Modeling the Reverse Bias & Breakdown	4.4,
	9	Mon	(02/10)	Zener Diodes, Applications: Better Voltage Regulator	
	10	Wed	(02/12)	Rectifier Circuits	4.5
	11	Fri	(02/14)	Applications: Rectifiers & DC Power Supplies	
MOSFETs	12	Mon	(02/17)	Applications: Limiters	4.6
	13	Wed	(02/19)	Semiconductors and the PN Junction	3,3.1-3.3
	14	Fri	(02/21)	Semiconductors and the PN Junction	3.4-3.5
	15	Mon	(02/24)	Engineering Expo	
	16	Wed	(02/26)	Exam 1 Review	
	17	Fri	(02/28)	MOSFET Intro, Device Structure & Operation	5, 5.1
	18	Mon	(03/03)	Catch-up Day	
	19	Wed	(03/05)	**Exam 1 Tentative Date**	
	20	Fri	(03/07)	Modes of Operation	5.2
	21	Mon	(03/10)	Mathematical Equations	5.2
	22	Wed	(03/12)	Circuit Analysis at DC	5.3
	23	Fri	(03/14)	The Common Source Transfer Function	7,7.1
			(03/15-23)	**Spring Break**	
	24	Mon	(03/24)	MOSFET Small Signal Analysis	7.2
	25	Wed	(03/26)	MOSFET Small Signal Analysis	
	26	Fri	(03/28)	Logic Intro, Digital Logic Inverters	14, 14.2
Digital Logic	27	Mon	(03/31)	NMOS & PMOS Inverter	
	28	Wed	(04/02)	Basic CMOS Logic Design	14.1
	29	Fri	(04/04)	CMOS Logic Inverter (In Depth)	14.3
	30	Mon	(04/07)	CMOS Logic Inverter (In Depth)	
	31	Wed	(04/09)	CMOS Inverter Dynamic Operation	14.4
	32	Fri	(04/11)	CMOS Transistor Sizing, Power Dissipation	14.5, 14.6
	33	Mon	(04/14)	CMOS Catch Up and Exam 2 Review	
	34	Wed	(04/16)	Sequential Logic: Basic Memory Element	16, 16.1
	35	Fri	(04/18)	**Exam 2 Tentative Date**	
BJTs	36	Mon	(04/21)	Latches and Flip Flops	16.2
	37	Wed	(04/23)	Memories	16.3
	38	Fri	(04/25)	BJTs Intro	6
	39	Mon	(04/28)	BJTs Intro, Operation	6.1
	40	Wed	(04/30)	BJTs Equations	6.2
	41	Fri	(05/02)	BJTs at DC	6.3
	42	Mon	(05/05)	BJT Common Emitter Transfer Function	7.1
	43	Wed	(05/07)	BJT Small Signal Analysis	7.2
		Fri	(05/09)	Stop Day	
		Thu	(05/15)	**Final 10:30am – 1:00pm**	