

EECS312-HW12v2: CMOS Logic Design

1. For the following logic functions:

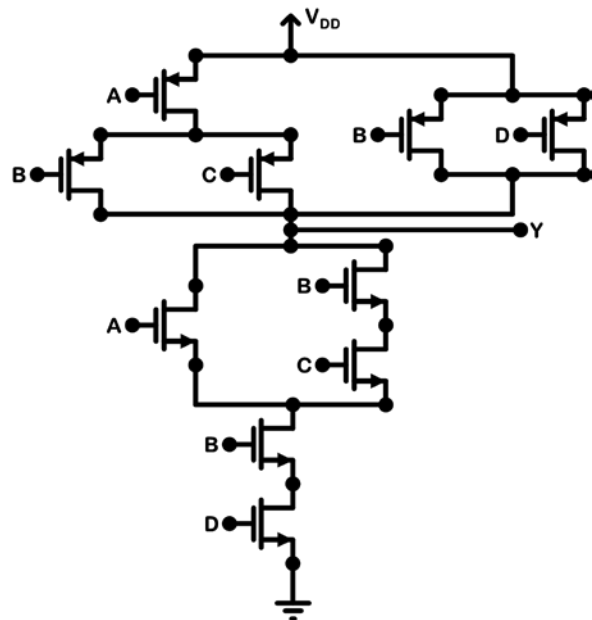
- Design the PUN and PDN.
- Identify the input combinations that the PUN will be conducting and for each combination determine the PUN resistance, r_{PUN} , in terms of r_{SDP} of a single PMOS component.
- Identify the input combinations that the PDN will be conducting and for each combination determine the PDN resistance, r_{PDN} , in terms of r_{DSN} of a single NMOS component.
- Using $k_n=k_p=4\text{mA/V}^2$, $V_{tn}=|V_{tp}|=1\text{V}$, and $V_{DD}=3\text{V}$, determine r_{DSN} and r_{SDP} .
- For an output capacitance of $C=50\text{pF}$, determine the maximum value of T_{PLH} and T_{PHL} .

$$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{D} \cdot \overline{B}$$

$$Y = \overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{C} + \overline{D} + \overline{B}$$

$$r = r_{DSN} = r_{SDP} = 1/((.004(3-0.8))) = 114\Omega$$

ABCD	r_{PUN}	r_{PDN}
0000	$(r+r/2) (r/2)$	open
0001	$(r+r/2) (r)$	open
0010	$(2r) (r/2)$	open
0011	$(2r) (r)$	open
0100	$(2r) (r)$	open
0101	(r)	open
0110	(r)	open
0111	open	$(4r)$
1000	$(r/2)$	open
1001	(r)	open
1010	$(2r)$	open
1011	(r)	open
1100	(r)	open
1101	open	$(3r)$
1110	(r)	open
1111	open	$(2r)+(r 2r)$



$$r_{PUN_MAX} = 2r = 228\Omega$$

$$r_{PDN_MAX} = 4r = 456\Omega$$

$$\tau_{PLH} = 50 \times 10^{-12} \cdot 228 \cdot \ln(2) = 8\text{ns}$$

$$\tau_{PHL} = 50 \times 10^{-12} \cdot 456 \cdot \ln(2) = 16\text{ns}$$

Sizes of PMOS: $(W/L)_{A, B1, C} = 2p$
 $(W/L)_{B2, D} = p$

Sizes of NMOS: $(W/L)_{B1, B2, C, D} = 4n$
 $(W/L)_A = 2n$

Could be simplified using the equation: $Y = \overline{A} \cdot \overline{C} + \overline{D} + \overline{B}$

$$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{D} + B$$

$$Y = \overline{B} \cdot (\overline{A} \cdot \overline{C} + \overline{D})$$

ABCD	r_{PUN}	r_{PDN}
0000	$r + (2r \parallel r)$	open
0001	$3r$	open
0010	$2r$	open
0011	open	$2r$
0100	open	r
0101	open	r
0110	open	r
0111	open	$r \parallel 2r$
1000	$2r$	open
1001	open	$2r$
1010	$2r$	open
1011	open	$r + r/2$
1100	open	r
1101	open	$r \parallel 2r$
1110	open	r
1111	open	$r \parallel (r + r/2)$

$$r_{\text{PUN_MAX}} = 3r = 342\Omega$$

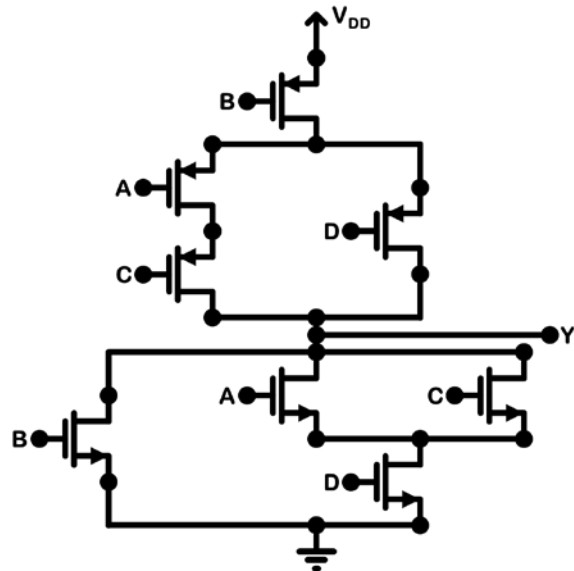
$$r_{\text{PDN_MAX}} = 2r = 228\Omega$$

$$\tau_{\text{PHL}} = 50 \times 10^{-12} \cdot 228 \cdot \ln(2) = 8\text{ns}$$

$$\tau_{\text{PLH}} = 50 \times 10^{-12} \cdot 342 \cdot \ln(2) = 12\text{ns}$$

Sizes of PMOS: $(W/L)_{A,B,C} = 3p$
 $(W/L)_D = 3p/2$

Sizes of NMOS: $(W/L)_{A,C,D} = 2n$
 $(W/L)_B = n$



2. A one-bit full adder with carry in/out has three inputs and two outputs.

Inputs:

A: First coefficient.

B: Second coefficient.

C_{IN}: Carry input from previous stage.

Outputs

S: Sum.

C_{OUT}: Carry output.

- a. Determine the logic functions for S and C_{OUT} in terms of A, B, and C_{IN}. Remember, for CMOS design you can only use ANDs, ORs, and NOTs in your logic functions.

Truth Table

A	B	C _{IN}	S	C _{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = /A \cdot /B \cdot C_{IN} + /A \cdot B \cdot /C_{IN} + A \cdot /B \cdot /C_{IN} + A \cdot B \cdot C_{IN}$$

$$S = /A \cdot /B \cdot C_{IN} + A \cdot B \cdot C_{IN} + /A \cdot B \cdot /C_{IN} + A \cdot /B \cdot /C_{IN}$$

$$S = C_{IN} \cdot (/A \cdot /B + A \cdot B) + /C_{IN} \cdot (/A \cdot B + A \cdot /B)$$

$$/S = /A \cdot /B \cdot /C_{IN} + /A \cdot B \cdot C_{IN} + A \cdot /B \cdot C_{IN} + A \cdot B \cdot /C_{IN}$$

$$/S = C_{IN} \cdot (A \cdot /B + A \cdot /B) + /C_{IN} \cdot (A \cdot B + /A \cdot /B)$$

$$C_{OUT} = /A \cdot B \cdot C_{IN} + A \cdot /B \cdot C_{IN} + A \cdot B \cdot /C_{IN} + A \cdot B \cdot C_{IN}$$

$$C_{OUT} = /A \cdot B \cdot C_{IN} + A \cdot /B \cdot C_{IN} + A \cdot B \cdot /C_{IN} + A \cdot B \cdot C_{IN} + A \cdot B \cdot C_{IN} + A \cdot B \cdot C_{IN}$$

$$C_{OUT} = (/A \cdot B \cdot C_{IN} + A \cdot B \cdot C_{IN}) + (A \cdot /B \cdot C_{IN} + A \cdot B \cdot C_{IN}) + (A \cdot B \cdot /C_{IN} + A \cdot B \cdot C_{IN})$$

$$C_{OUT} = (B \cdot C_{IN}) + (A \cdot C_{IN}) + (A \cdot B)$$

$$C_{OUT} = C_{IN} \cdot (A + B) + A \cdot B$$

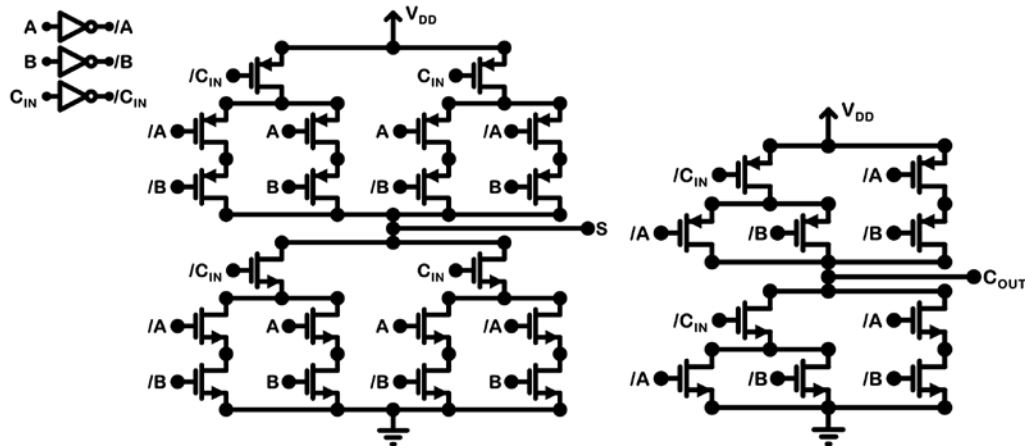
$$/C_{OUT} = /A \cdot /B \cdot /C_{IN} + /A \cdot /B \cdot C_{IN} + /A \cdot B \cdot /C_{IN} + A \cdot /B \cdot /C_{IN}$$

$$/C_{OUT} = (/A \cdot /B \cdot /C_{IN} + /A \cdot /B \cdot C_{IN}) + (/A \cdot /B \cdot /C_{IN} + /A \cdot B \cdot /C_{IN}) + (A \cdot /B \cdot /C_{IN} + /A \cdot /B \cdot /C_{IN})$$

$$/C_{OUT} = (/A \cdot /B) + (/A \cdot /C_{IN}) + (/B \cdot /C_{IN})$$

$$/C_{OUT} = /A \cdot /B + /C_{IN} \cdot (/A + /B)$$

b. Implement the each logic function in CMOS.



c. Determine how many PMOS and NMOS transistors are required.

Inverters: 3PMOS, 3NMOS
Sum: 10PMOS, 10NMOS
Carry: 5PMOS, 5NMOS
Total: 18PMOS, 18NMOS

d. Using $k_n=k_p=20\text{mA/V}^2$, $V_{tn}=|V_{tp}|=0.8\text{V}$, and $V_{DD}=2.5\text{V}$, determine r_{DSN} , r_{SDP} .

$$r_{DSN} = r_{SDP} = 1/ (.02(2.5-.8)) = 30\Omega$$

e. For an output capacitance of $C=40\text{pF}$, determine the maximum propagation delay for carry output, C_{OUT} , based on the maximum PUN or PDN resistance.

$$\tau_{PHL} = \tau_{PLH} = 40 \times 10^{-12} \cdot (2 \cdot 30) \cdot \ln(2) = 1.7\text{ns}$$

f. What would the maximum net delay be for an 8-bit inverter and resulting maximum clock rate?

$$\text{delay} = 8 \cdot \tau_P = 13\text{ns}$$

$$f_{\text{MAX}} = 1/13\text{ns} = 75\text{MHz}$$

note: If you need to use an inverter to satisfy the function syntax for the PUN or PDN, just use the inverter symbol in part b and assume (1 PMOS and 1 NMOS) per inverter in part c, and assume the inverter has zero propagation delay for parts e & f.