Semiconductor Memories

Semiconductor Memory:
- Semiconductor memory is a fundamental component of digital systems from large computers to embedded microprocessors.

Types of Memories:
- In any given system, there are typically various types of memory that are used to perform different functions such as:
  - Storing instructions
  - Storing data

- Memory can be divide into two broad categories depending on **access time**.
  - The time needed to retrieve data from a particular memory location.

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<th>Memory</th>
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<th>Speed</th>
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<tr>
<td>DRAM</td>
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<td>Moderate</td>
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<td>Serial</td>
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<td>Slow</td>
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</table>
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- **Main Memory:**
  - Usually referred to as *random access memory (RAM)*.
  - The time required to access a given part of memory is independent of the memory location.
  - Typical volatile – looses contents when power is cut.

- **Mass-Storage Memory:**
  - Usually referred to as *serial* or *sequential memory* (disks or tapes), although flash storage is becoming more the norm for personal computers.
  - Typically non-volatile, retains contents.
  - Data are available only in the sequence that the data were stored.
  - The time required to access a given part of memory is dependent on the memory location.
  - Average access time is typically much longer than that of random access memory.
Memory can also be classified by whether it is **read/write** or **read-only** memory.

**Read/Write Memory (RAM):**
- data can be stored and retrieved with relatively the same access time.
- RAM can be classified even more by Static RAM (SRAM) and Dynamic RAM (DRAM).

**Read-Only Memory (ROM):**
- has similarly fast retrieve times but restricted writing operations.
- employed in function that require table look-ups.
- employed in video game cartridges.
- low-level computer input/output or **Basic Input/Output System (BIOS)**.
Semiconductor Memories

- Review and comparison of different types of memories.

<table>
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<th>Volatile</th>
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<td>Dynamic RAM</td>
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MEMORY

- Random Access
- Mass Storage
- RAM
- ROM
- Dynamic
- Static
- Serial
- Disk
- Tape
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Memory-Chip Organization:

- **Random-access memory** is typically organized into a two-dimensional grid \((2^M \text{ by } 2^N)\) of cells that each store a single bit.

  - \(2^M\) refers to the number of address lines (number of rows).
  - \(2^N\) refers to the number of bits per address line (number of columns).
  - A single address line is referred to as a **word line**.

- The bits are addressable (accessed) either individually \((N = 0)\) or more generally in groups of powers of 2 \((N = 0, 1, 2, 3, 4, \ldots)\).
Example:

Consider 128 kbit block of memory that is byte addressable.

We all know that byte refers to a group of 8 bits (N=3).

The total number of address lines is 128 kbit / 8 = 128*1024/8 = 16384 = 2^{14}.

The memory requires a 14-bit address to retrieve a word line (M=14).

What if it is addressable in groups of 64 bits (N=6).

The total number of address lines is 128 kbit / 64 = 2048 = 2^{11}.

This memory would require an 11-bit address.

For both of these cases N+M=17.
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Let’s look at this organization as a figure:

- **Memory Cell** – a single bit of the memory block.
- **M** – the number of address bits required by the *row decoder*.
- **$2^N$** – Width of the output word.
- **Word Line** – a single row of the memory block addressed by the row decoder.
  - each word line contains $2^N$ bits.
  - there are a total of $2^M$ word lines.
- **Bit Lines (Digit Line)** – a single column of the memory block.
  - Input and output data lines
Random Access Memory (RAM) Cells

The RAM Memory Cell (bit):

- **Connections** – Each memory cell has 3 to 4 connections:
  - 1. The **word line** is attached to the output of **row decoder** and is used to **select** (activate or connect) **a row of cells**.
    - This is an **input only** to the memory cell.
    - when **high connects** the **row** of cells to the **bit lines & write enable**.
Random Access Memory (RAM) Cells

The RAM Memory Cell (bit):

- **Basic Operation** – the word line selects a memory row and activates the access transistor(s) providing an active connection to the bit lines.

- **Structure** – the structure of the memory cell depends on the type of RAM, which can be either **static (SRAM)** or **dynamic (DRAM)**.
Random Access Memory (RAM) Cells

Static Random Access Memory (SRAM):
- Utilize static latches as the storage mechanism.
- A basic configuration for this static memory bit is:
  - the **memory component**: the simple CMOS clocked Latch (~16 Transistors)
  - the **input/output component**: 2 access transistors.
  - **And gate** for **write enable**: 8 transistors.
  - Total of **26 Transistors** per bit.

**The SRAM Read Operation:**
- the read operation is non-destructive and the data is retained.

**The SRAM Write Operation:**
- The bit lines are charge to VDD or 0 depending on what is written.
Random Access Memory (RAM) Cells

Dynamic Random Access Memory (DRAM):

- Utilize capacitors as the storage mechanism.
- A basic configuration is a capacitor attached to the bit lines via an access transistor.
  - the **memory component**: a capacitor.
  - the **input/output component**: an access transistor.
- Capacitors discharge (there is no getting around this) so the DRAM memory cell must be periodically recharged by performing a read operation and then writing this data back into the memory.

**The DRAM Read Operation**

- the read operation is destructive and the data is lost from the cell. This cell is refreshed by what was read.
- the read operation must also include a write operation.

**The DRAM Write Operation**

- The bit lines are charge to VDD or 0 depending on what is written.
Random Access Memory (RAM) Cells

Comparisons between SRAM and DRAM.

**Advantages of DRAM**
- Less Complex
- Less Space
- Less Cost

**Advantages of SRAM**
- Faster
- Lower Power
- No refresh is required
- Non-destructive read operation
Random Access Memory (RAM) Cells

Address Decoder

Operation

- For M address bits, there will be $2^M$ possible word lines.
- Each word line is a combinational logic function of the M inputs:
  - For M=8 (pull down n equations)
    - $\text{not}(y_0) = M_2 + M_1 + M_0$
    - $\text{not}(y_1) = M_2 + M_1 + \text{not}(M_0)$
    - $\text{not}(y_2) = M_2 + \text{not}(M_1) + M_0$
    - $\text{not}(y_3) = M_2 + \text{not}(M_1) + \text{not}(M_0)$
    - ...
- there will be $2^3$ equation each requiring 3 Transistors for the PDN and 3 for the PUN, plus 3 inverters (6 Transistors)
- In General, the Address Decoder will have a Total of $2^M * 2^M + 2^M$ Transistor.