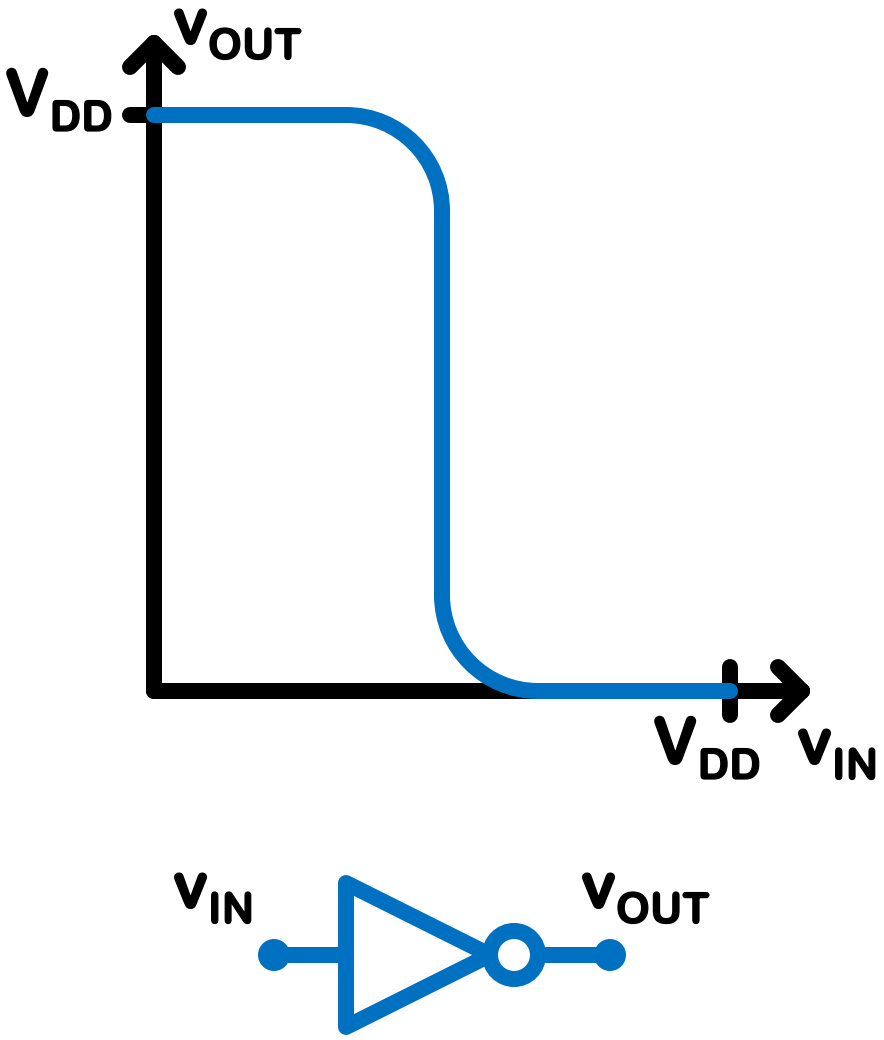
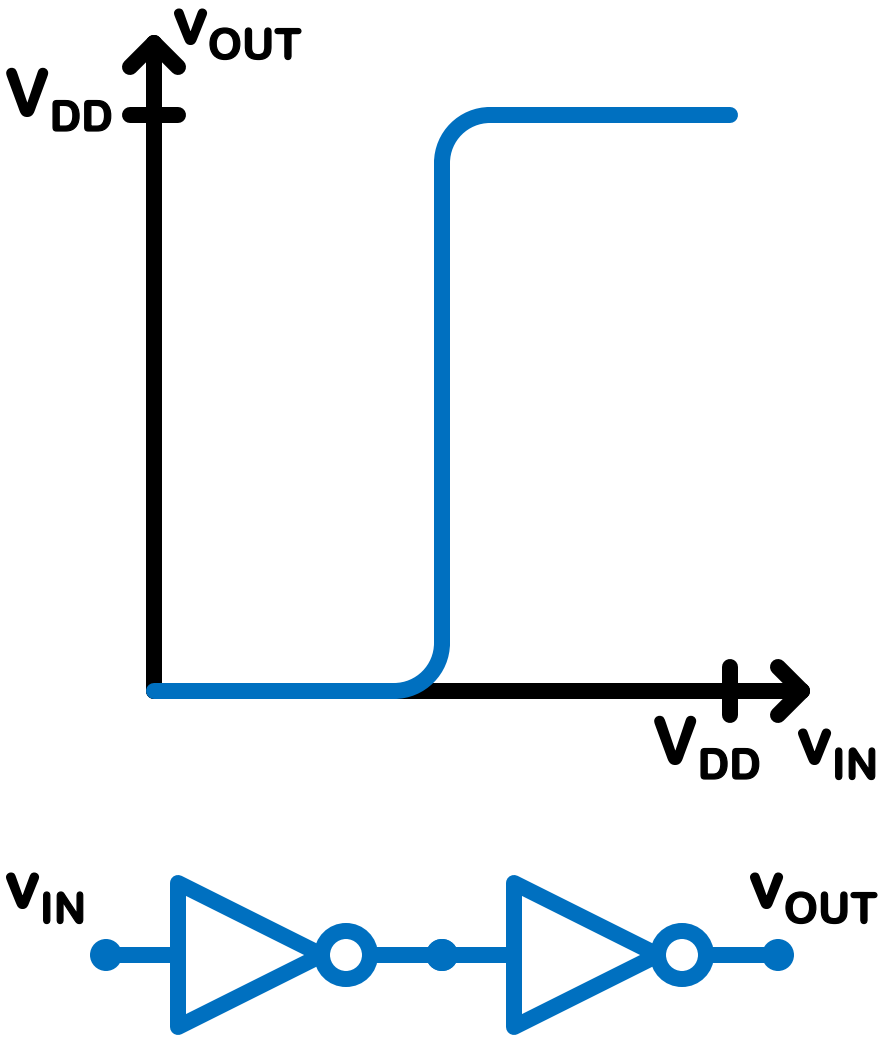
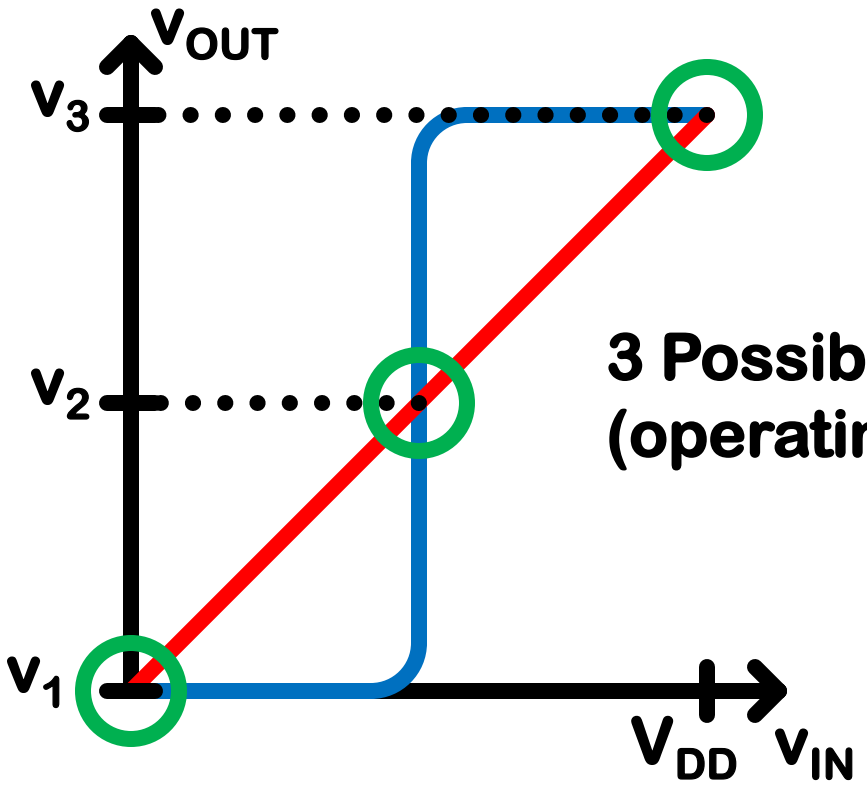
Sequential Logic: Inverter and Transfer Function



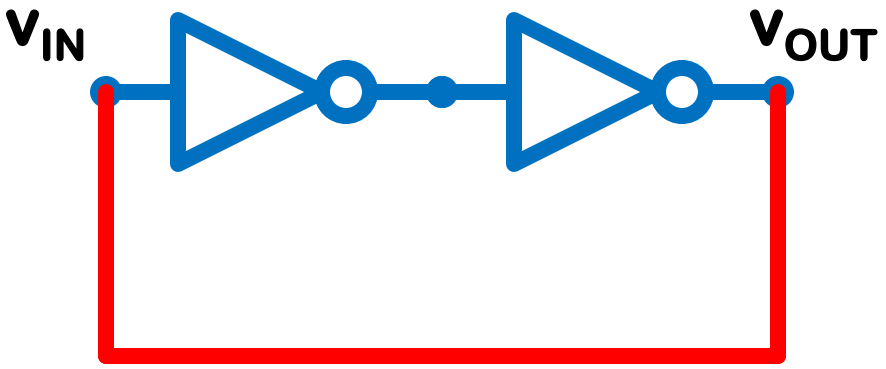
Two Inverters in Series



Two Inverters in Series with Feedback

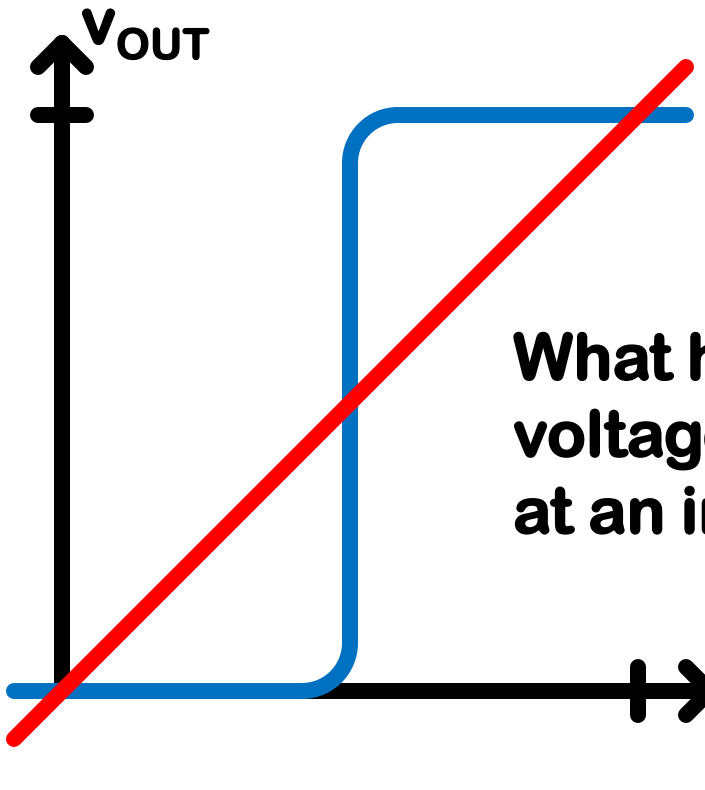


3 Possible Solutions
(operating points).

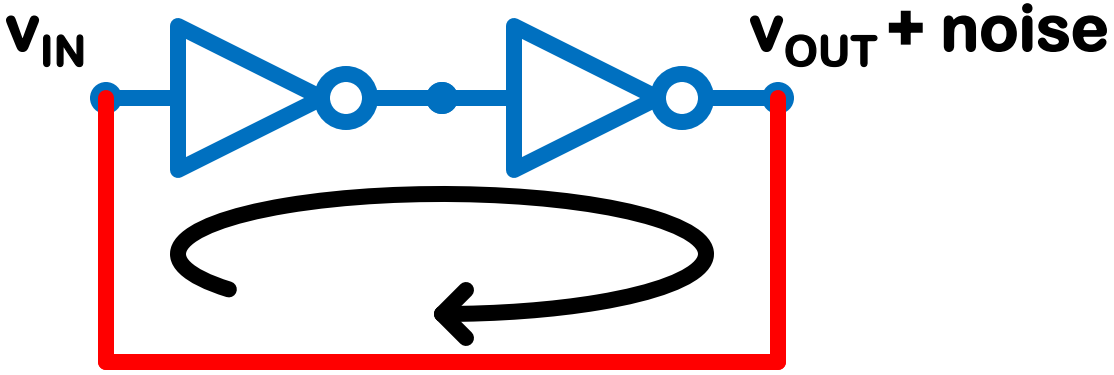


Two Inverters in Series with Feedback (with noise)

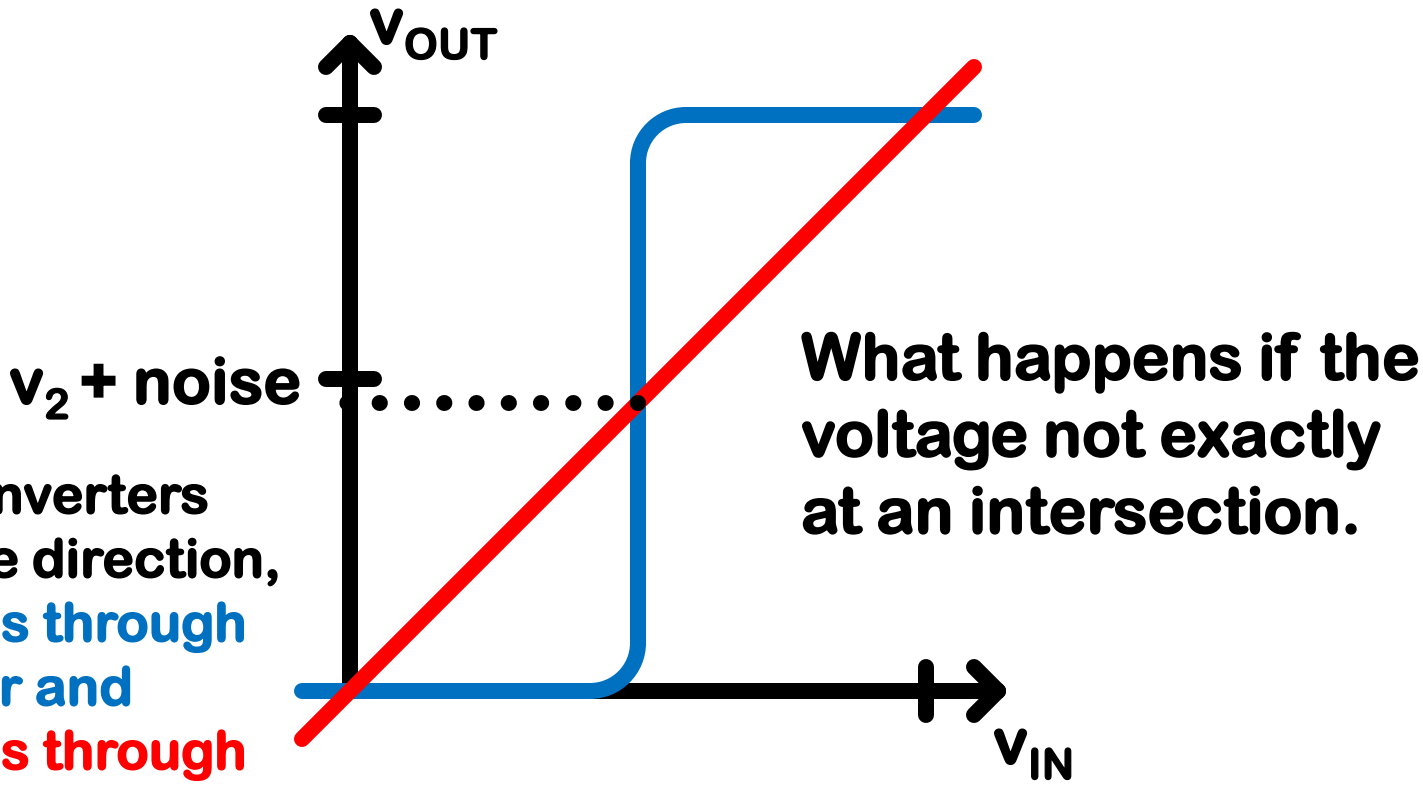
Since the inverters work in one direction, v_{IN} to v_{OUT} is through the inverter and v_{OUT} to v_{IN} is through the feedback.



What happens if the voltage not exactly at an intersection.



Two Inverters in Series with Feedback (with noise)



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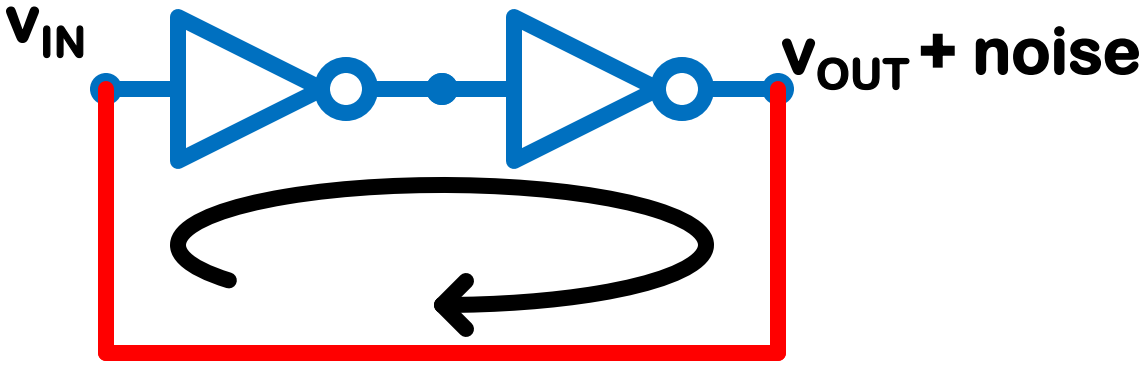
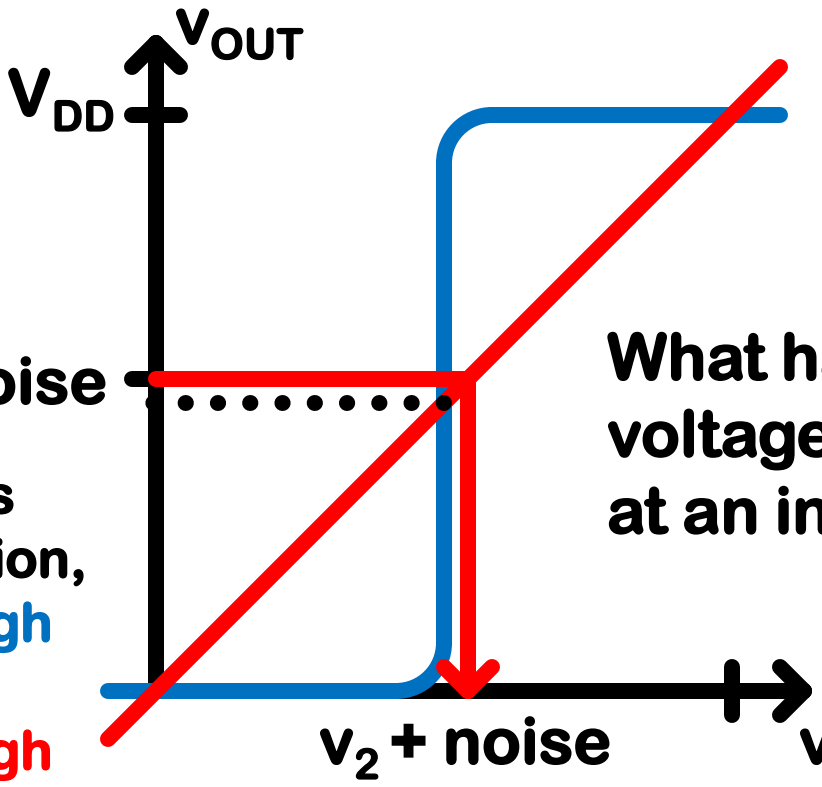


Two Inverters in Series with Feedback (with noise)



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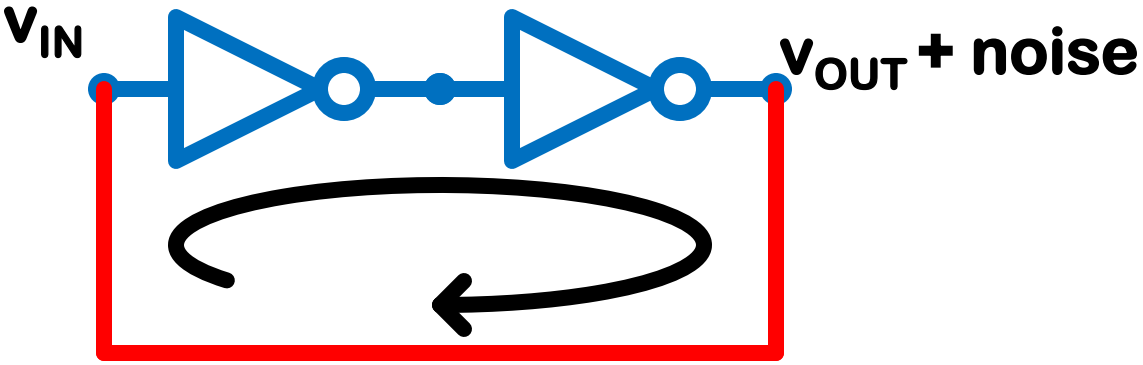
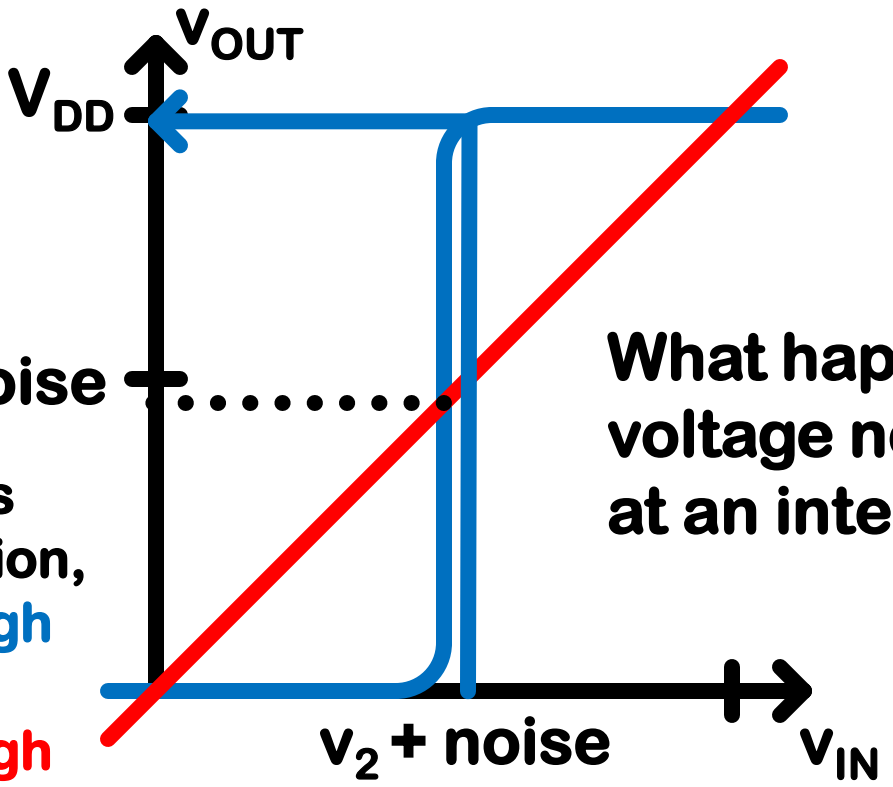


Two Inverters in Series with Feedback (with noise)



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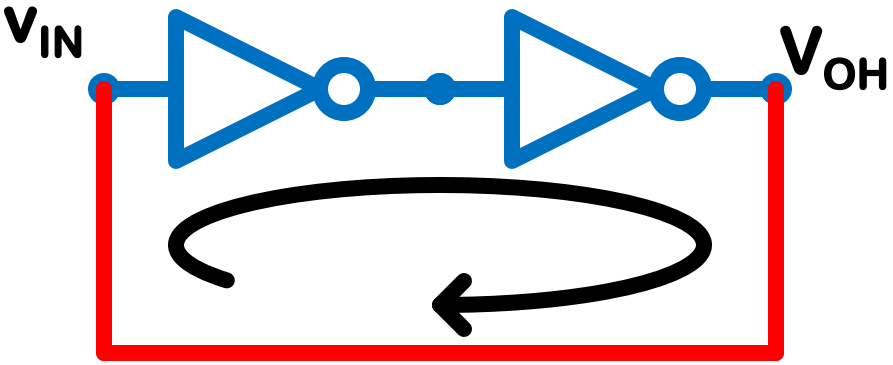
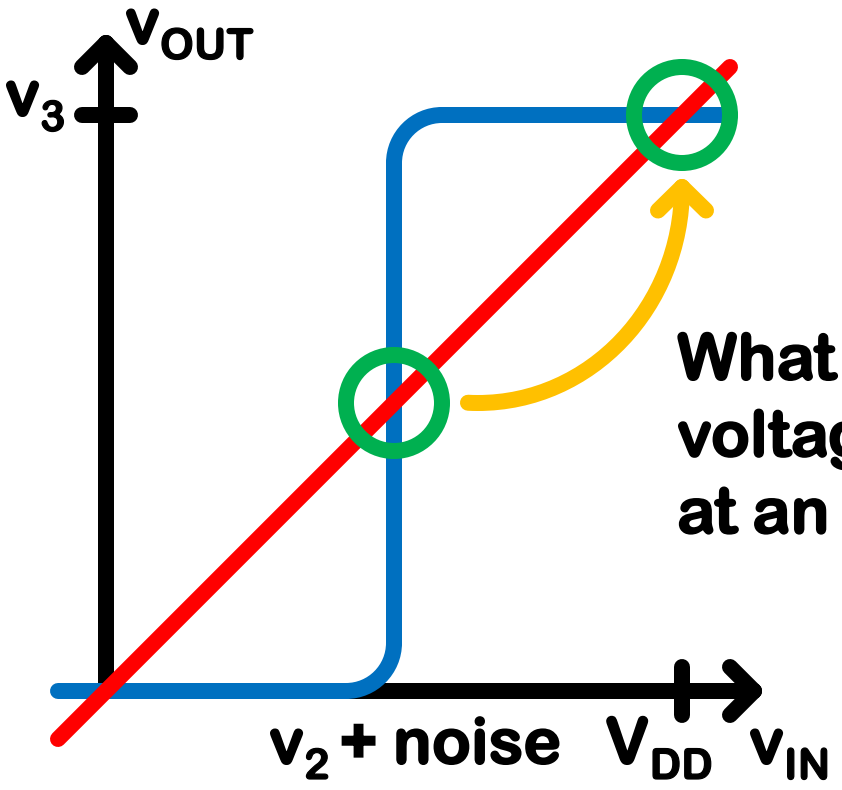


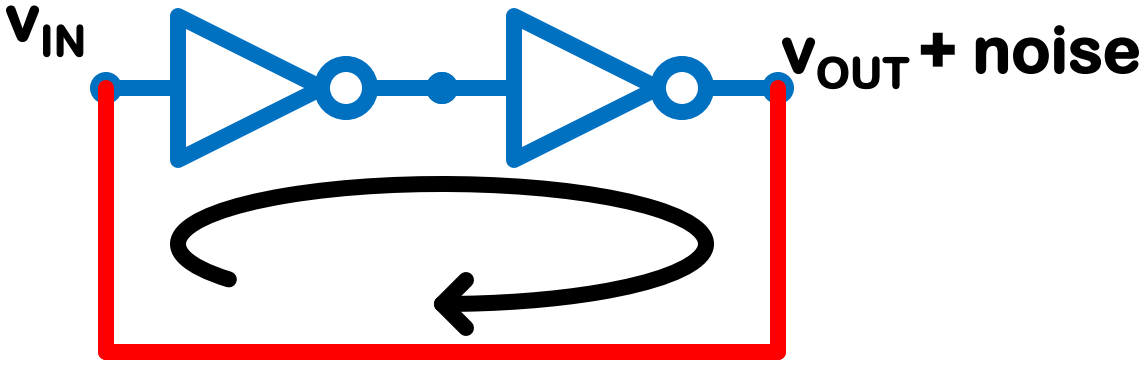
Two Inverters in Series with Feedback (with noise)

If v_{OUT} is at v_2, a very small amount of positive noise will push v_{OUT} to $v_3=V_{OH}$, and negative noise will push v_{OUT} to $v_1=V_{OL}$.

The circuit will not stay at v_2 as this operating point is unstable.



What happens if the voltage not exactly at an intersection.



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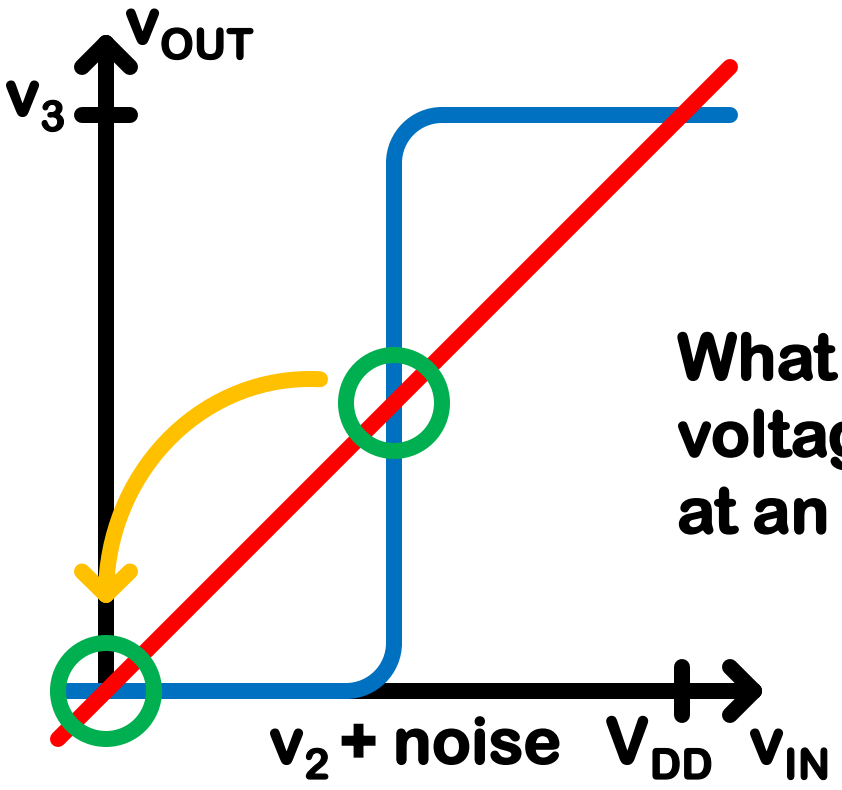

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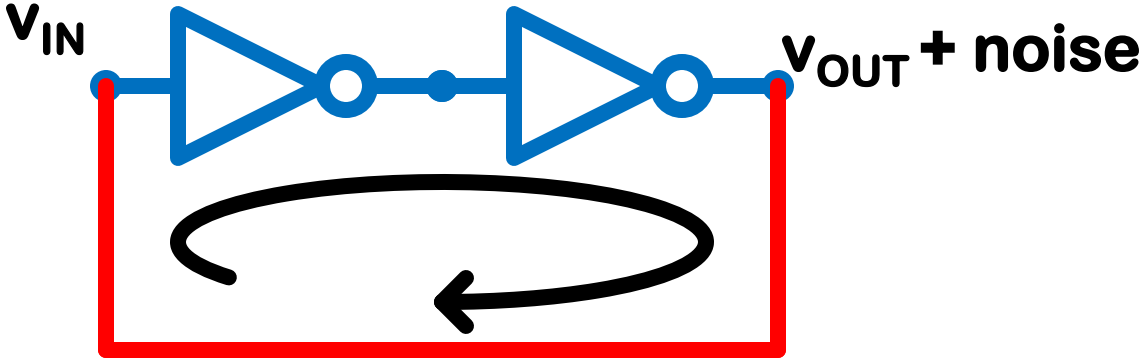

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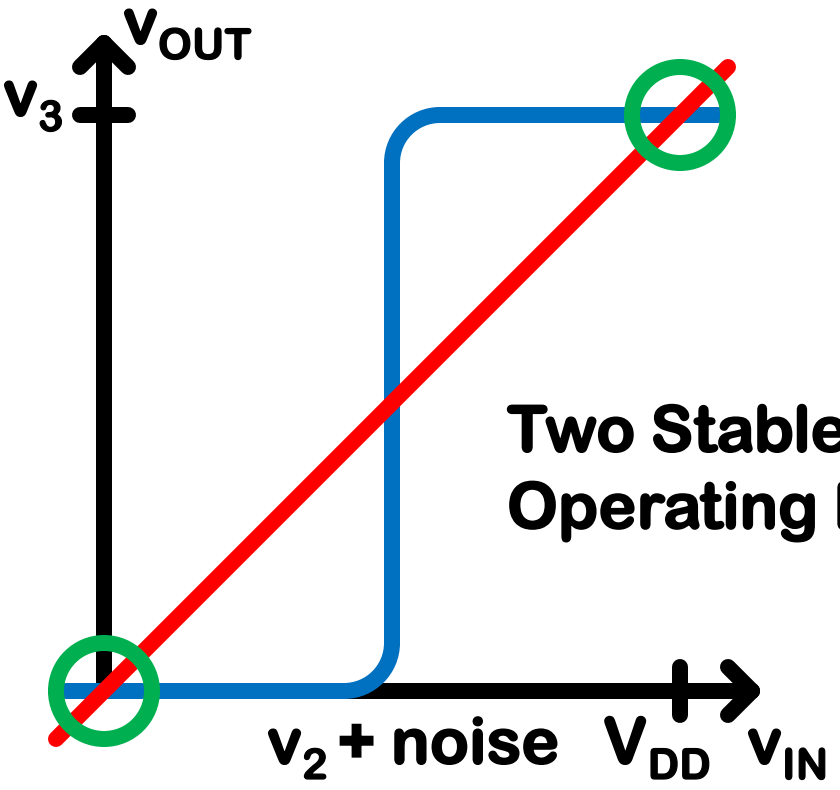
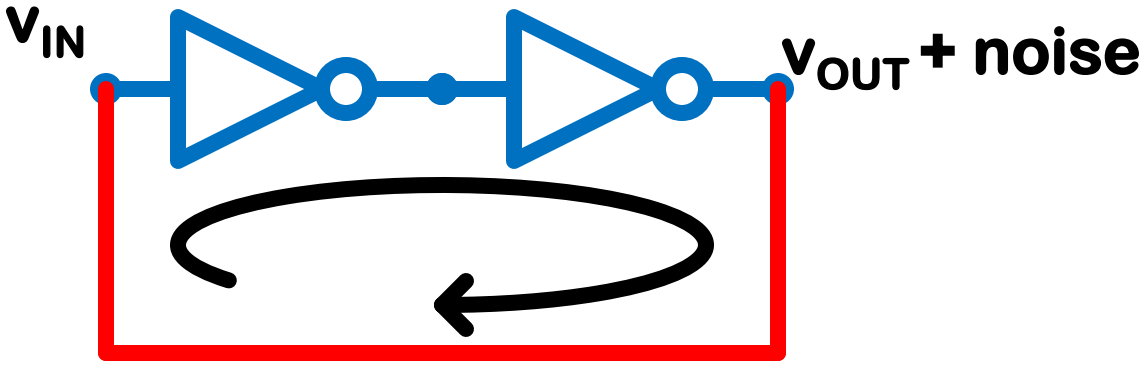
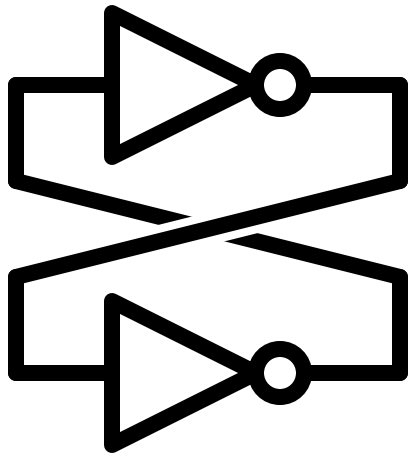


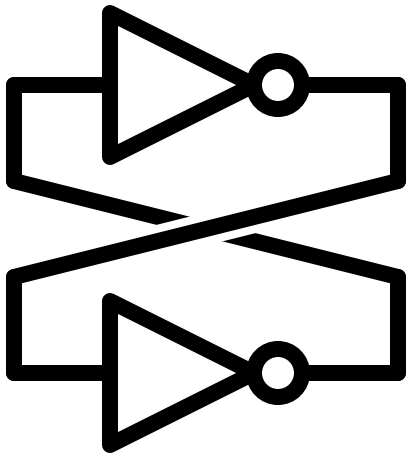


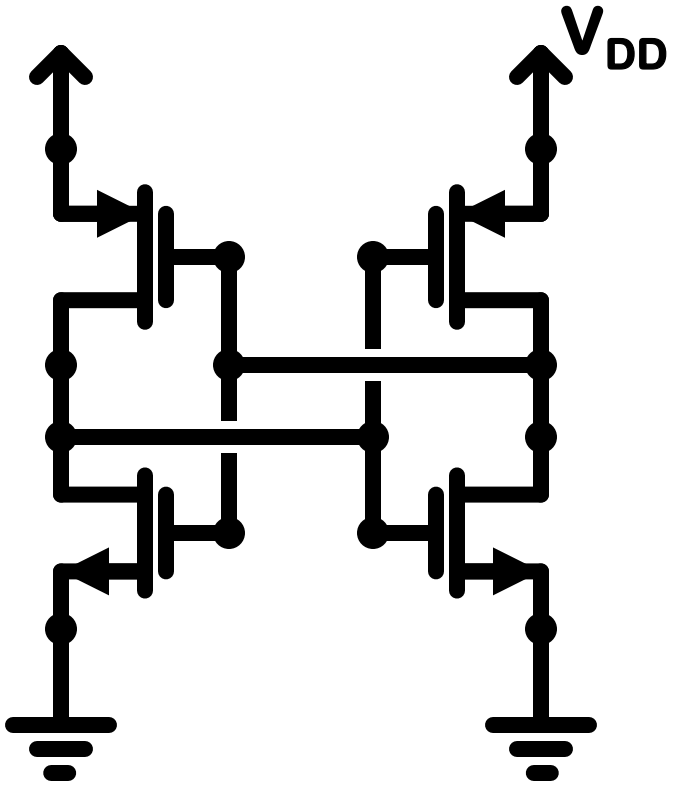
Cross-Coupled Inverters: Basic Static Memory Element



Pro: Once set, it will hold its value (logic high or low) without an input.
Con: There are no inputs.

Cross-Coupled Inverters: Basic Static Memory Element





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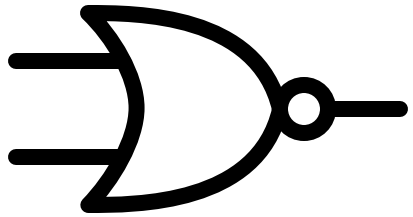
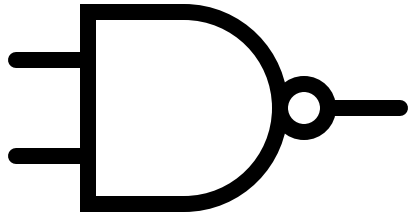
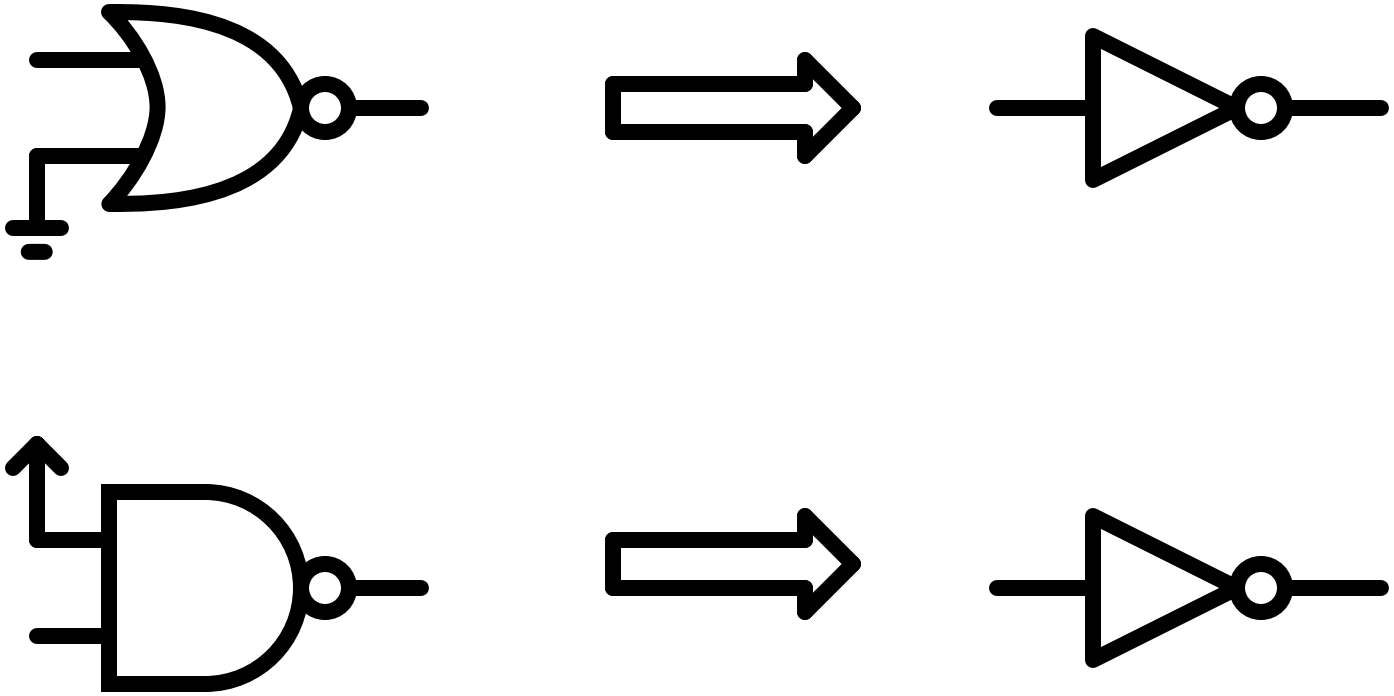
Cross-Coupled Inverters: Basic Static Memory Element





Adding inputs with NOR or NAND gate.
NOR: if one input is low, it behaves as an inverter.
NAND: if one input is high, it behaves as an inverter.

Cross-Coupled Inverters: Basic Static Memory Element



Adding inputs with NOR or NAND gate.
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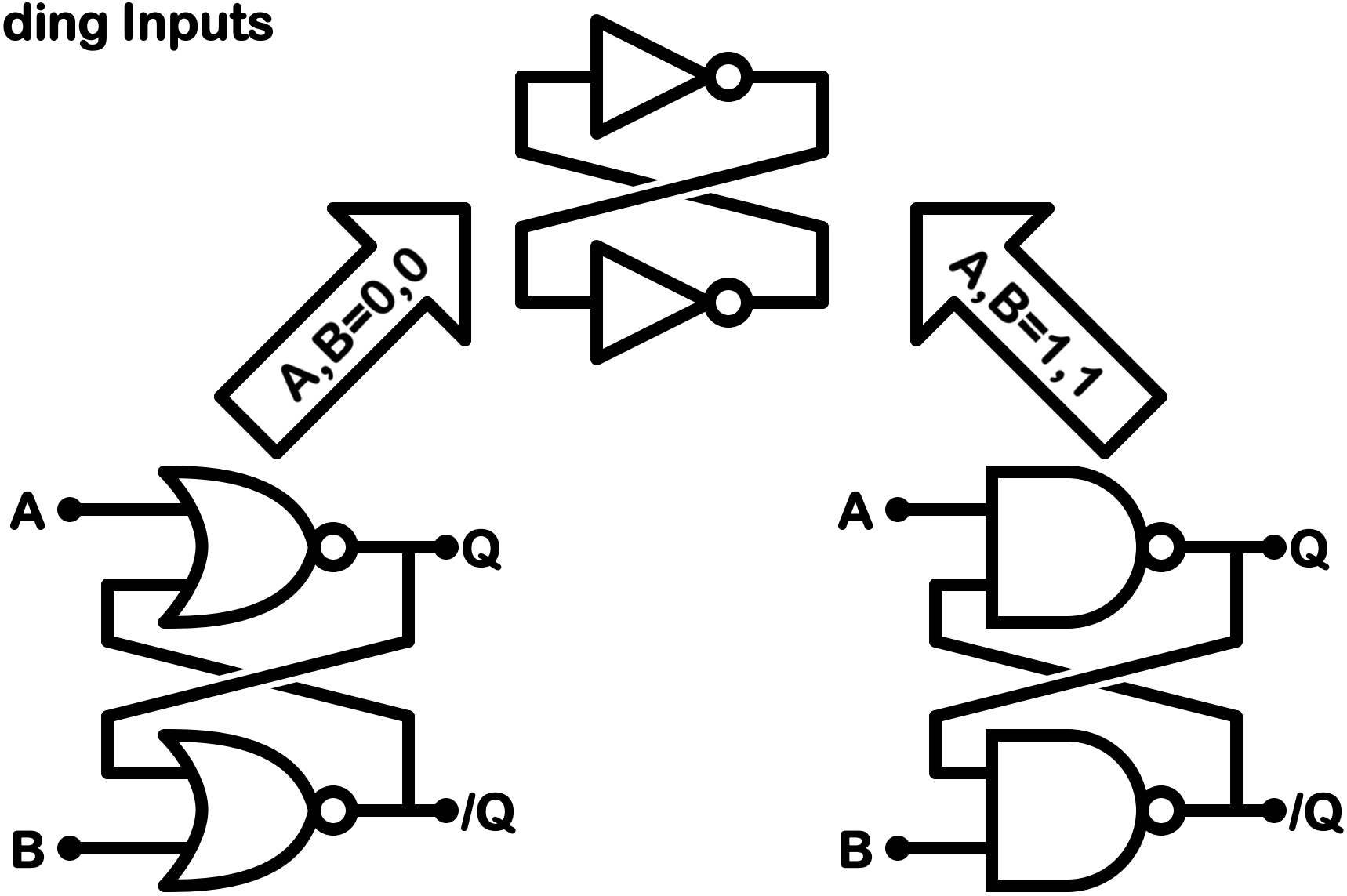
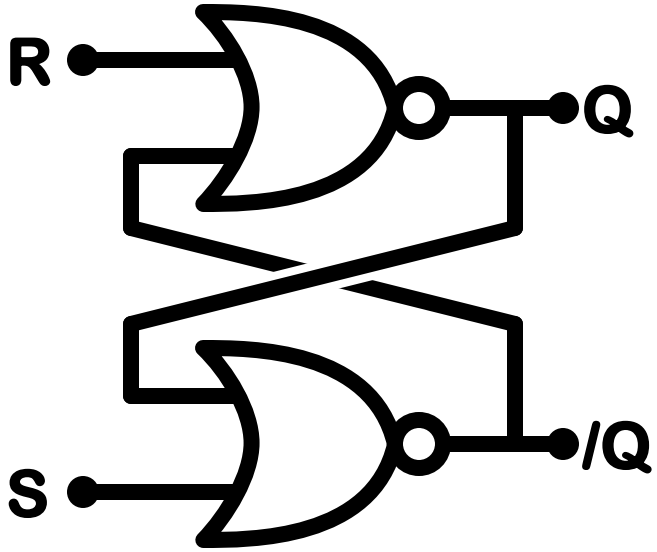
Adding Inputs

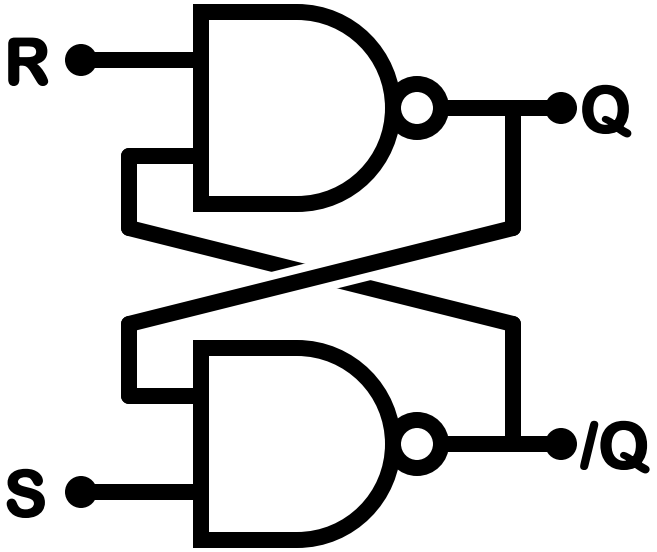


SR Latch

S	R	Q	/Q
0	0	Q	/Q
0	1	0	1
1	0	1	0
1	1	0	0

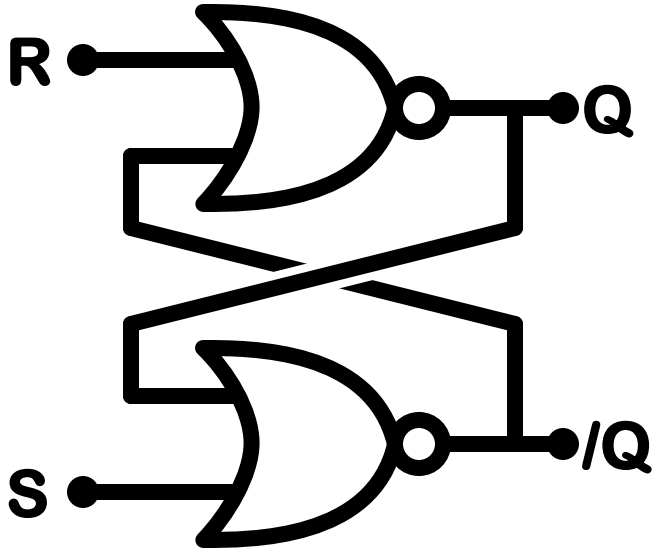


S	R	Q	/Q
0	0	1	1
0	1	0	1
1	0	1	0
1	1	Q	/Q

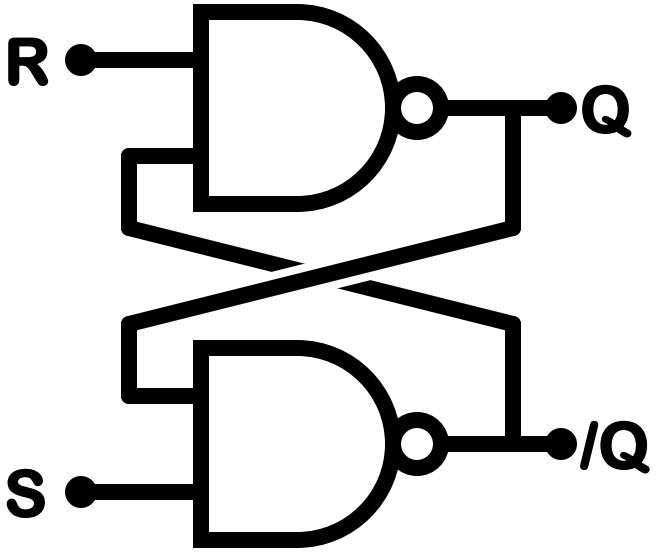


SR Latch: Adding Combinational Logic For a D-Latch

S	R	Q	/Q
0	0	Q	/Q
0	1	0	1
1	0	1	0
1	1	0	0



S	R	Q	/Q
0	0	1	1
0	1	0	1
1	0	1	0
1	1	Q	/Q



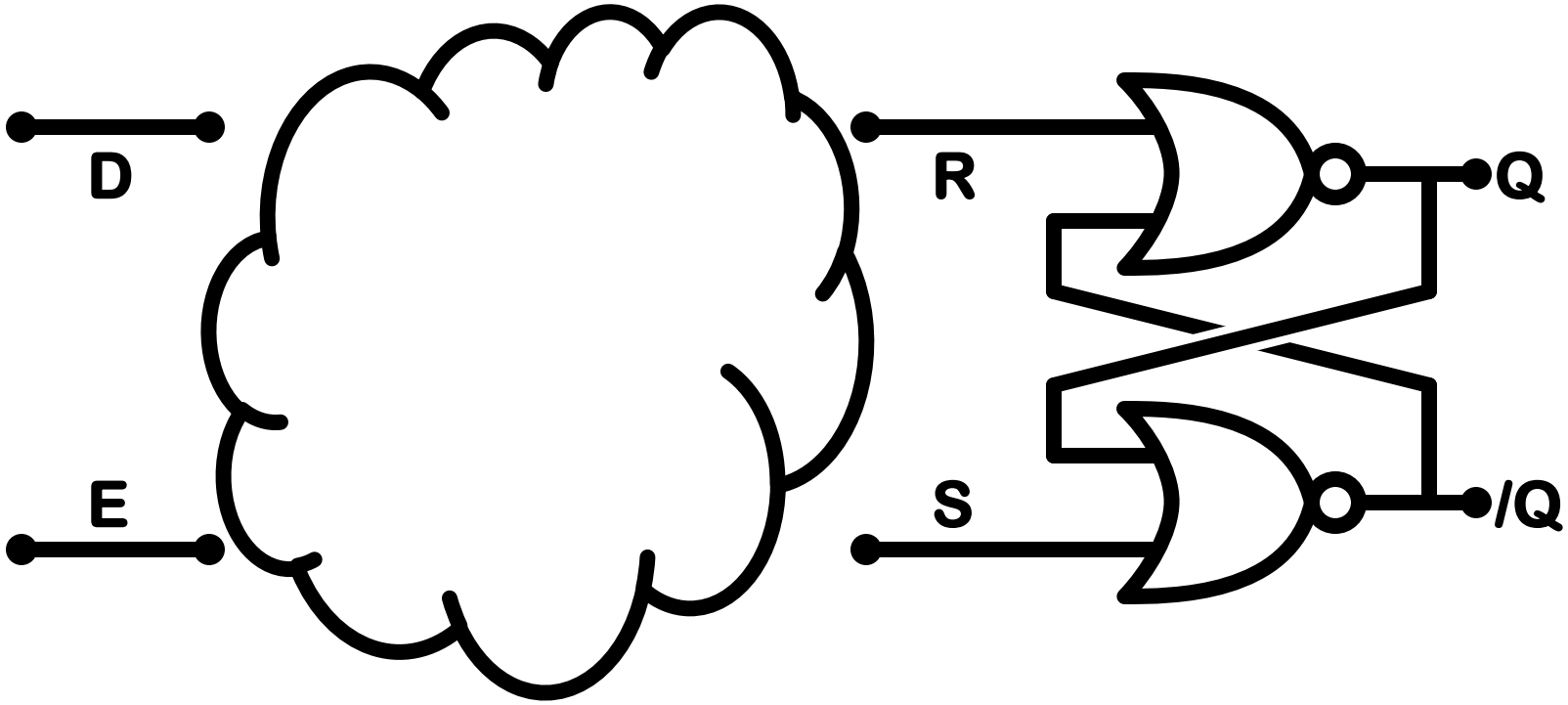
SR Latch: Adding Combinational Logic For a D-Latch

D	E	S	R
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

$S = D \cdot E$

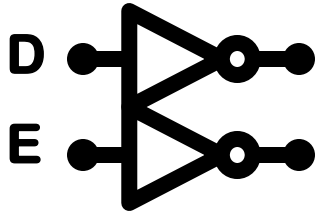
$R = /D \cdot E$

S	R	Q	/Q
0	0	Q	/Q
0	1	0	1
1	0	1	0
1	1	0	0



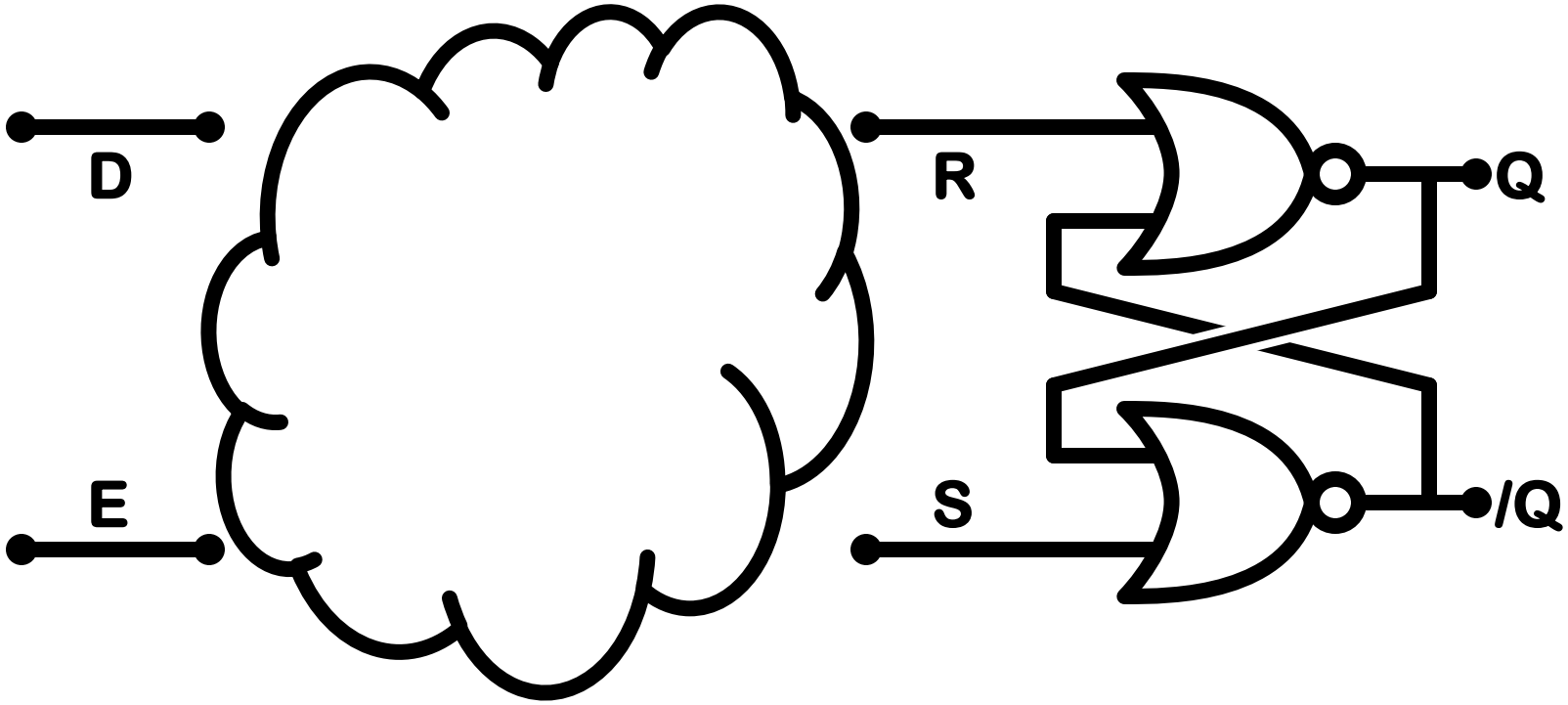
SR Latch: Adding Combinational Logic For a D-Latch

D	E	S	R
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0



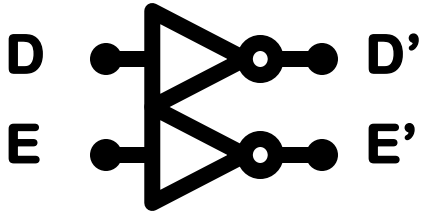
S = /D'·/E' NOR
R = /D·/E' NOR

S	R	Q	/Q
0	0	Q	/Q
0	1	0	1
1	0	1	0
1	1	0	0



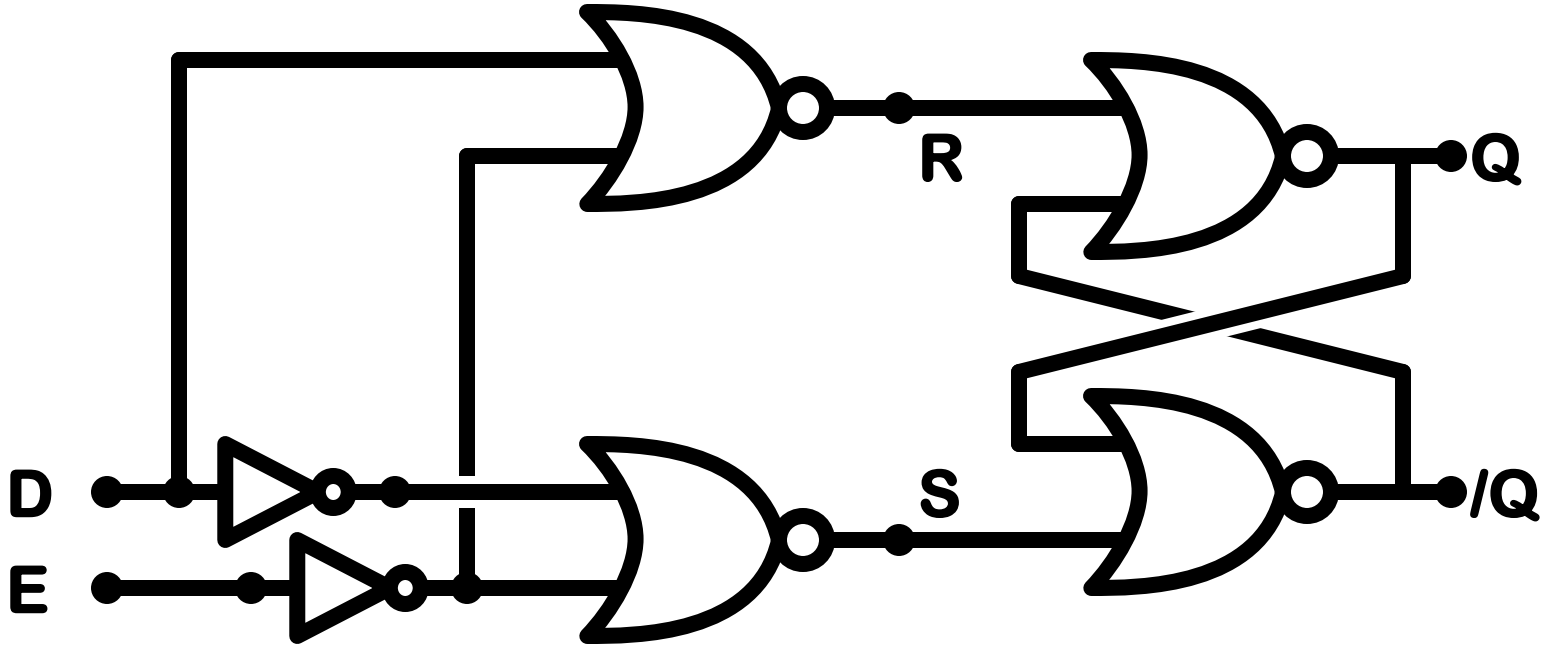
SR Latch: Adding Combinational Logic For a D-Latch

D	E	S	R
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0



S = /D'·/E' NOR
R = /D·/E' NOR

S	R	Q	/Q
0	0	Q	/Q
0	1	0	1
1	0	1	0
1	1	0	0

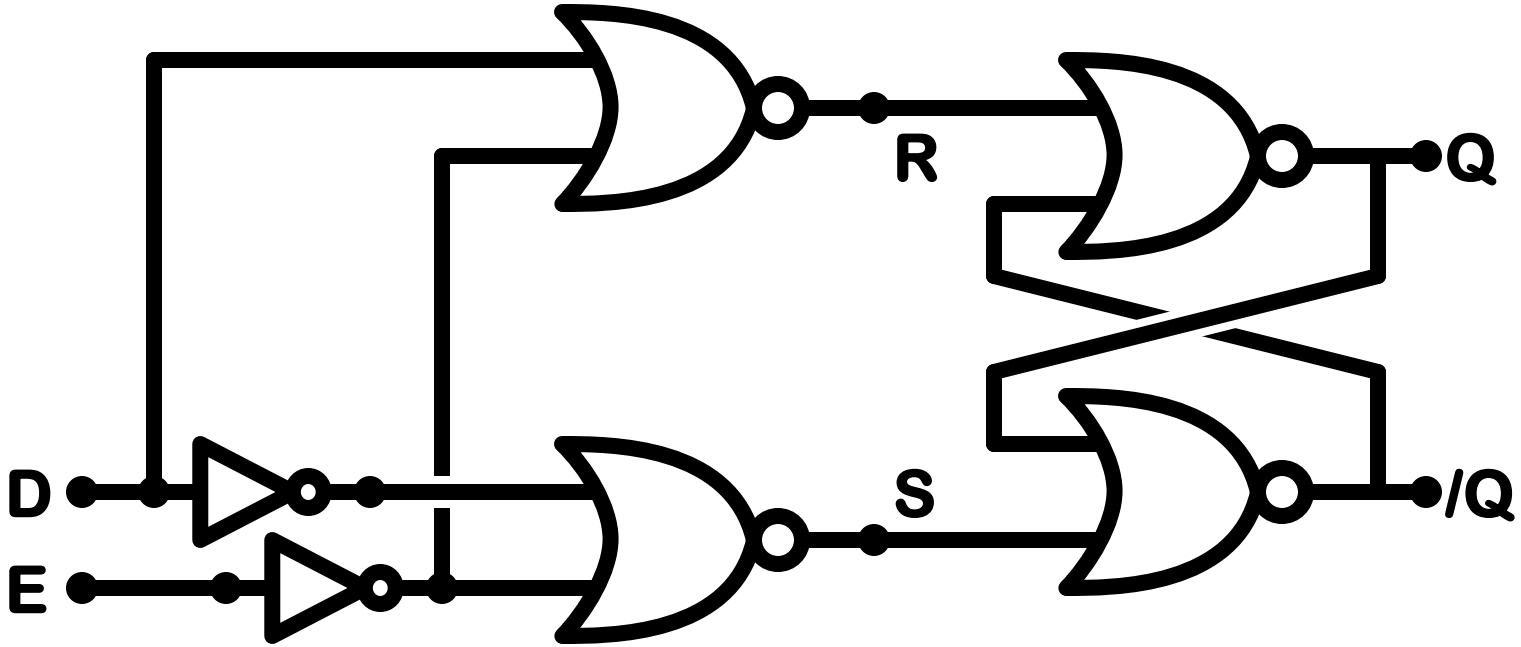


SR Latch: Adding Combinational Logic For a D-Latch

D	E	Q	/Q
0	0	Q	/Q
0	1	0	1
1	0	Q	/Q
1	1	1	0

2 Inverters: 4 Trans.
4 NOR: 16 Trans.

20 Transistors.



SR Latch: Adding Combinational Logic For a D-Latch

D	E	S	R
0	0	1	1
0	1	0	1
1	0	1	1
1	1	1	0

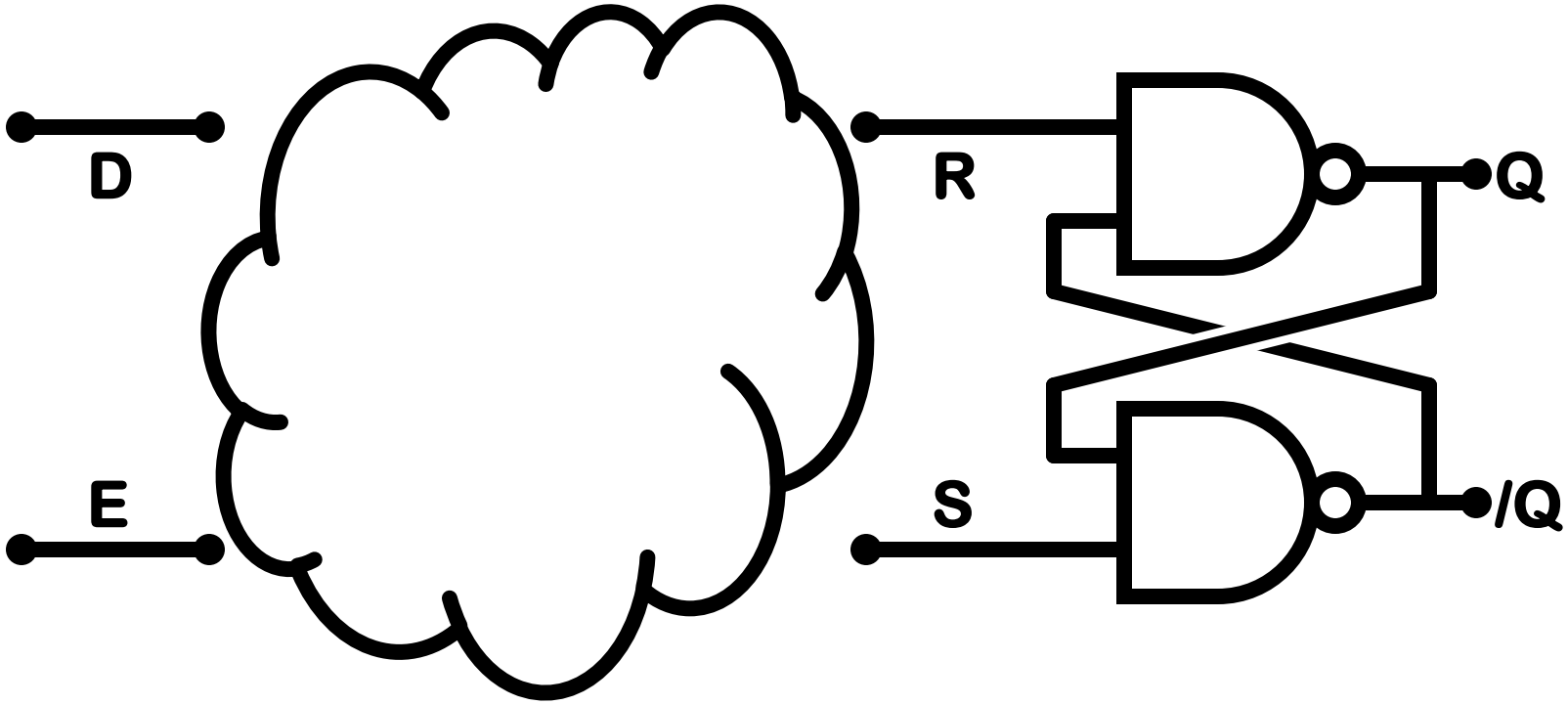
/S = /D·E

/R = D·E; NAND

Can you show that

/S = R·E; NAND

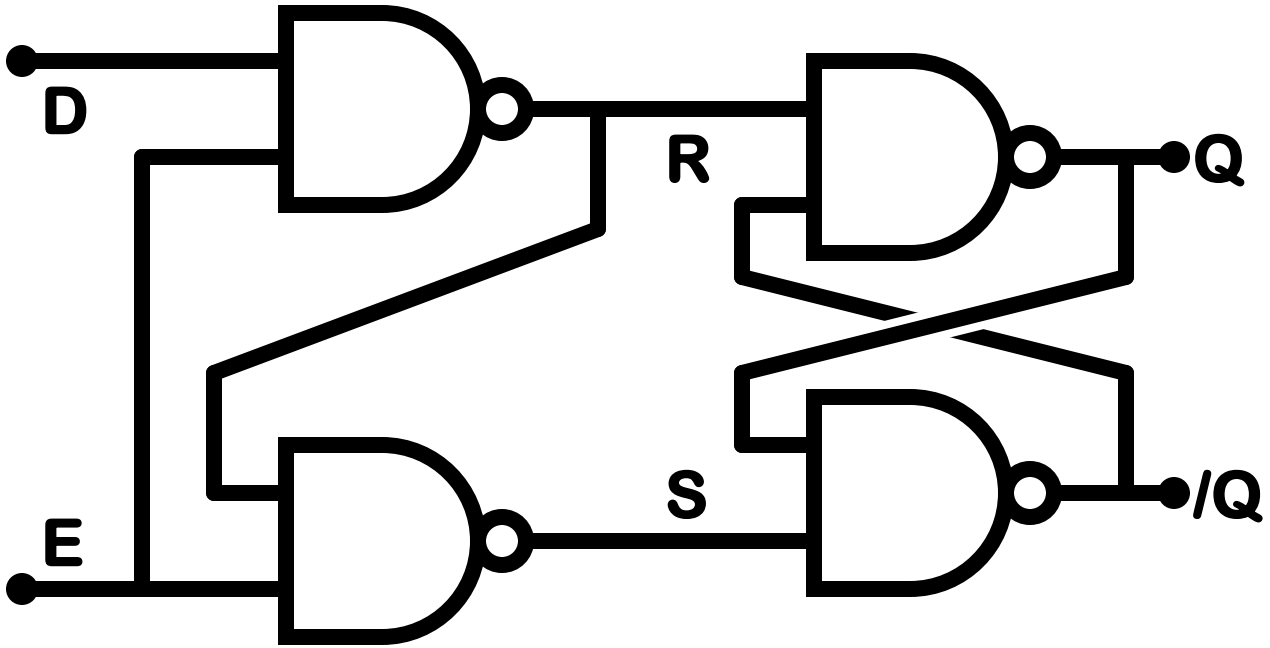
S	R	Q	/Q
0	0	1	1
0	1	0	1
1	0	1	0
1	1	Q	/Q



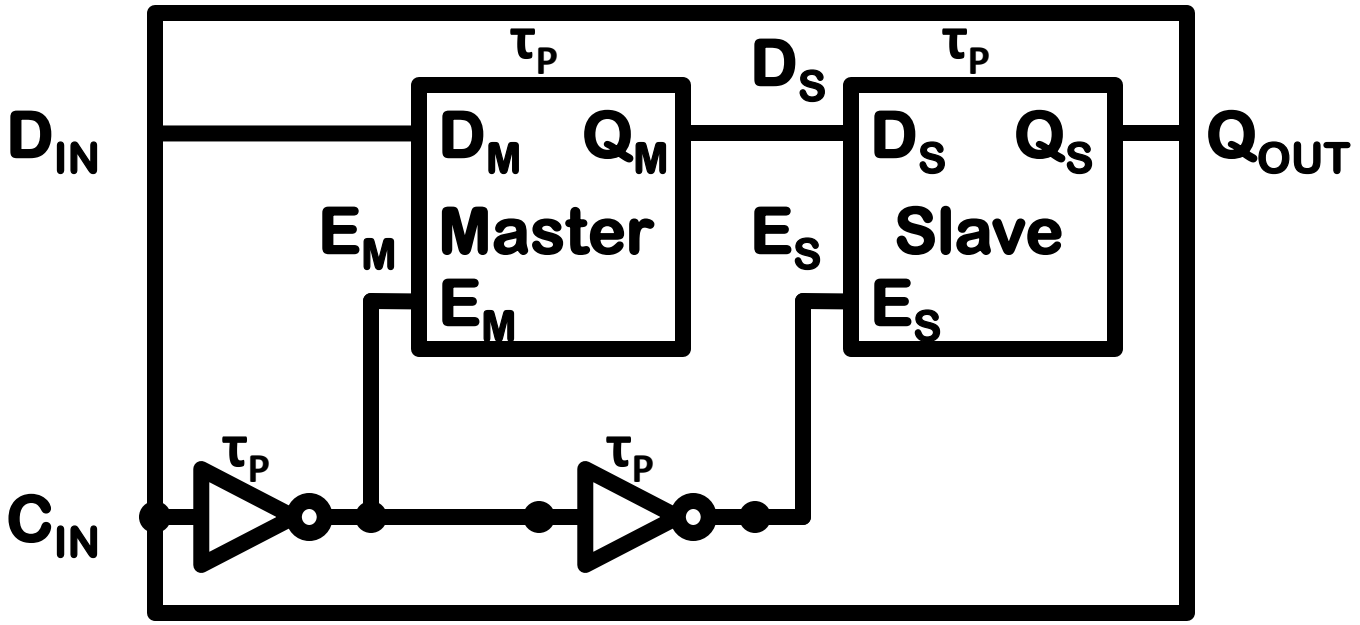
SR Latch: Adding Combinational Logic For a D-Latch

D	E	Q	/Q
0	0	Q	/Q
0	1	0	1
1	0	Q	/Q
1	1	1	0

4 NAND Gates,
16 Transistors



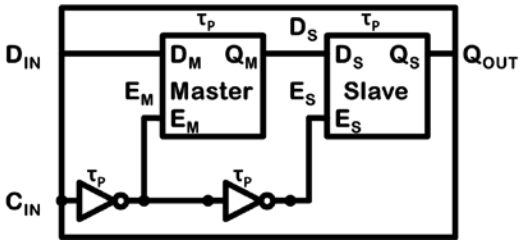
The D-Flip Flop … Edge Triggered



2x D-Latch: 32~40 Transistors

2x Inverter: 4 Transistors

The D-Flip Flop … Edge Triggered



D_{IN} D_0 D_1

Q_M, D_S D_0 D_1

Q_{OUT} D_0 Output Available D_1

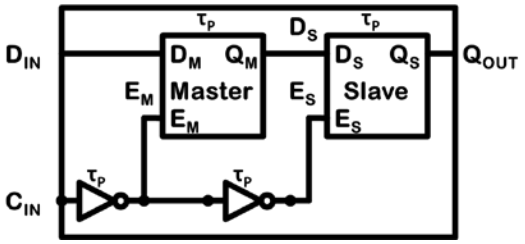
C_{IN} Rising Edge

E_M Data Latched

E_S Output Latched

τ_P τ_P

The D-Flip Flop … Edge Triggered



D_{IN} D_0 D_1

Q_M, D_S D_0 D_1

Q_{OUT} D_0 Output Available D_1

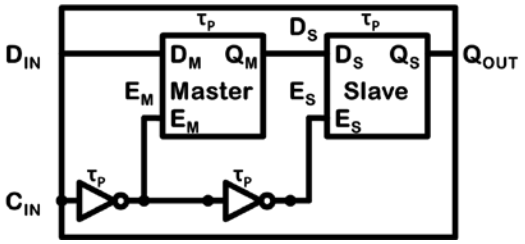
C_{IN} Rising Edge

E_M Data Latched

E_S Output Latched

τ_P τ_P

The D-Flip Flop … Edge Triggered



D_{IN} D_0 ? D_1

Q_M, D_S D_0 ? D_1

Q_{OUT} D_0 Output Available D_1

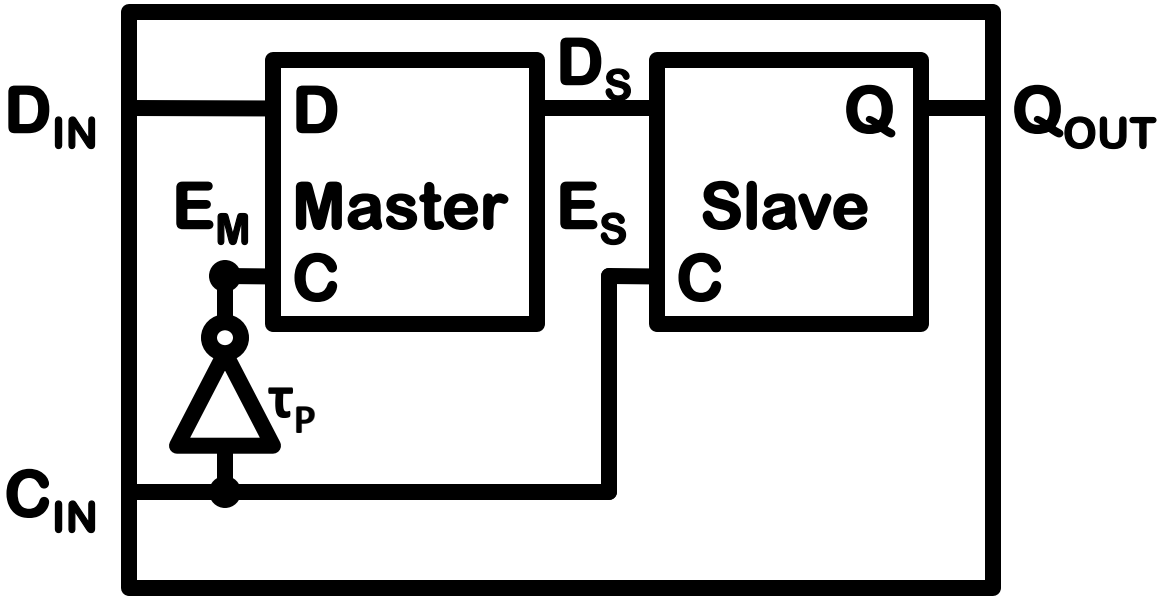
C_{IN} Rising Edge

E_M Data Latched

E_S Output Latched

τ_P τ_P

The D-Flip Flop … Edge Triggered



2x D-Latch: 32~40 Transistors
1x Inverter: 2 Transistors

The D-Flip Flop … Edge Triggered