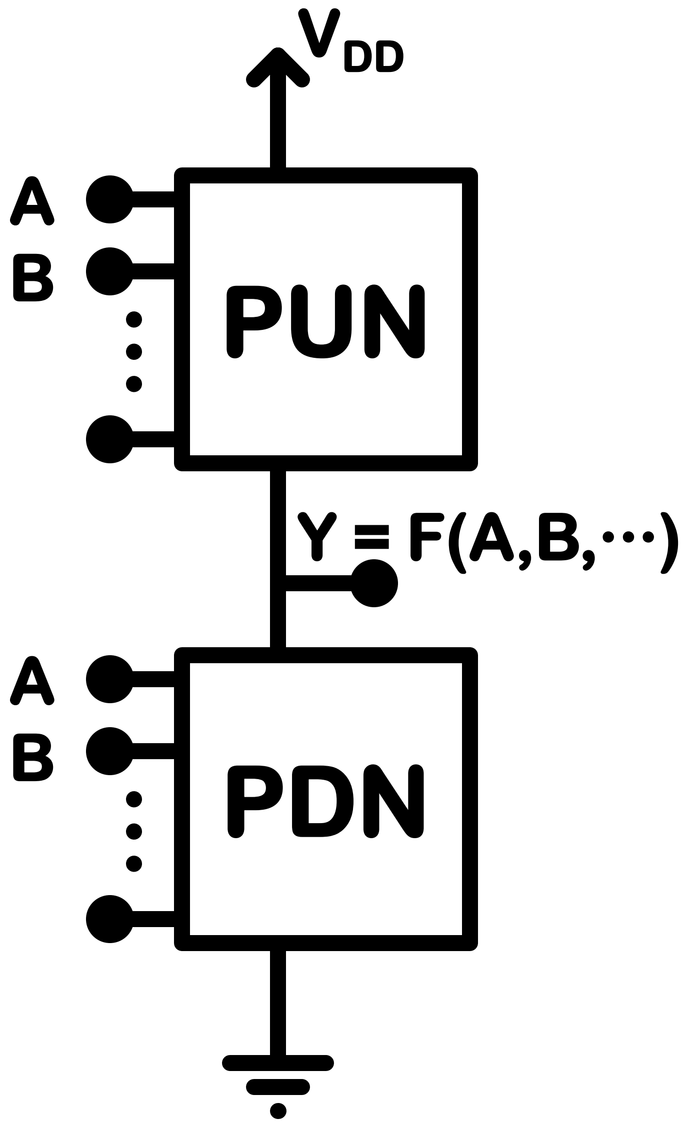
Combinational Logic Design



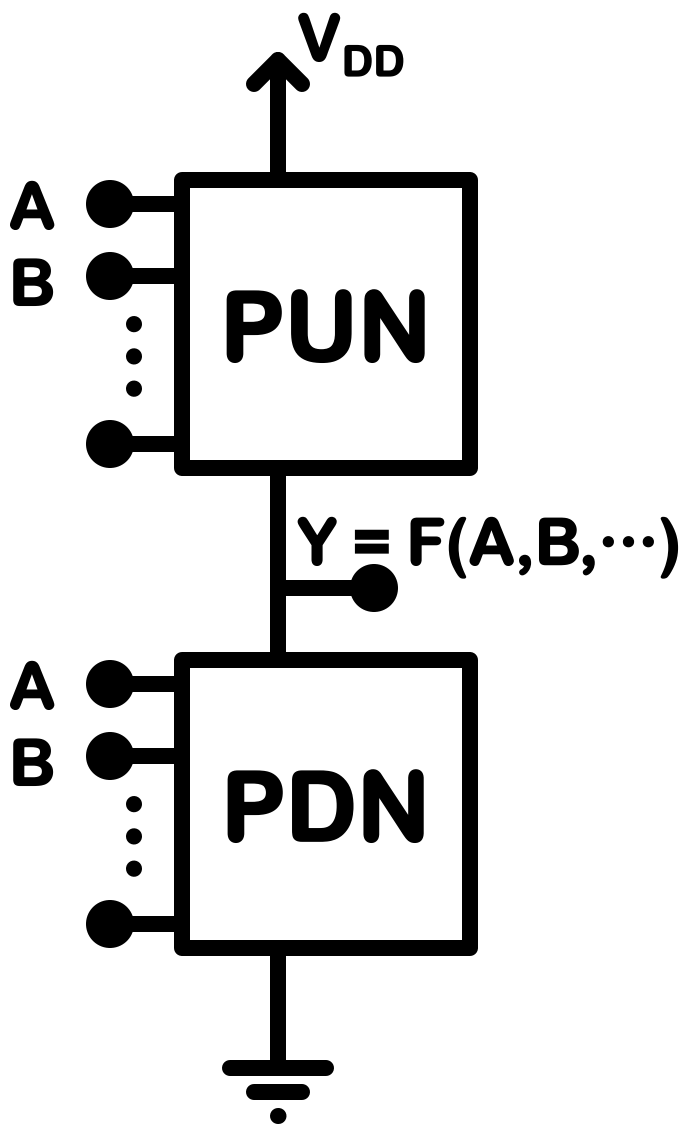
Two Complementary Networks

Pull Up Network (PUN):

- Conducting (ties the output Y high) when the Function (F) result in logic True (1).
- Open when the Function (F) result in logic False (0).
- Constructed with PMOS devices.
- PMOS are conducting when the input (gate voltage) is Low or False (0).
- Prefer the Function (F) to be expressed as:

$$Y = F_{PUN}(\overline{A}, \overline{B}, \cdots)$$

Combinational Logic Design



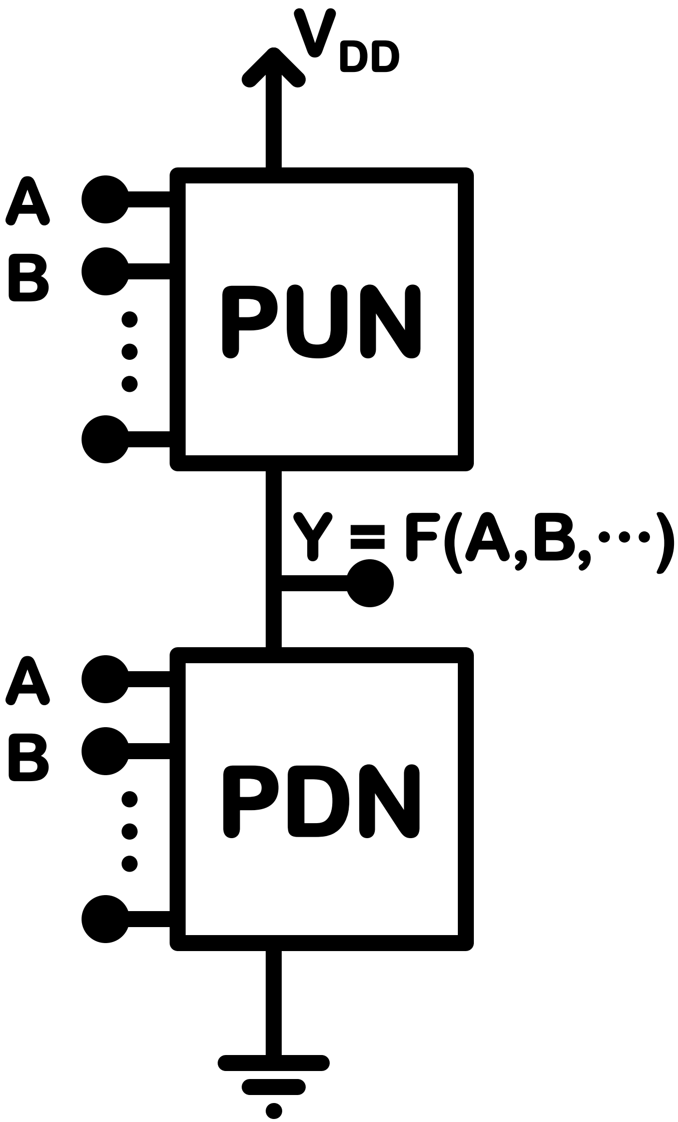
Two Complementary Networks

Pull Down Network (PDN):

- Conducting (ties the output Y low) when the Function (F) result in logic False (0).
- Open when the Function (F) result in logic True (1).
- Constructed with NMOS devices.
- NMOS are conducting when the input (gate voltage) is High or True (1).
- Prefer the Function (F) to be expressed as:

$$Y = \overline{F_{PDN}(A, B, \cdots)}$$

Combinational Logic Design

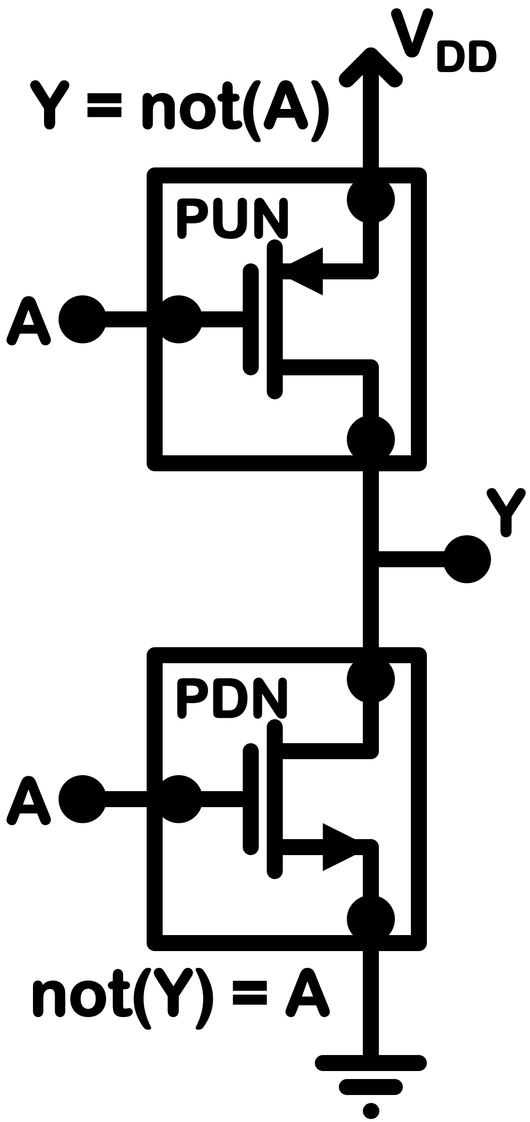


Two Complementary Networks

Other Notes:

- Networks must be complementary:
  When PUN is conducting, PDN is open.
  When PDN is conducting, PUN is open.
- Both open would leave Y floating.
- Both conducting would dissipate more power and leave Y in transition region.
- $\overline{F_{PDN}(A,B,\cdots)} = F_{PUN}(\overline{A},\overline{B},\cdots) = F(A,B,\cdots)$

Combinational Logic Design

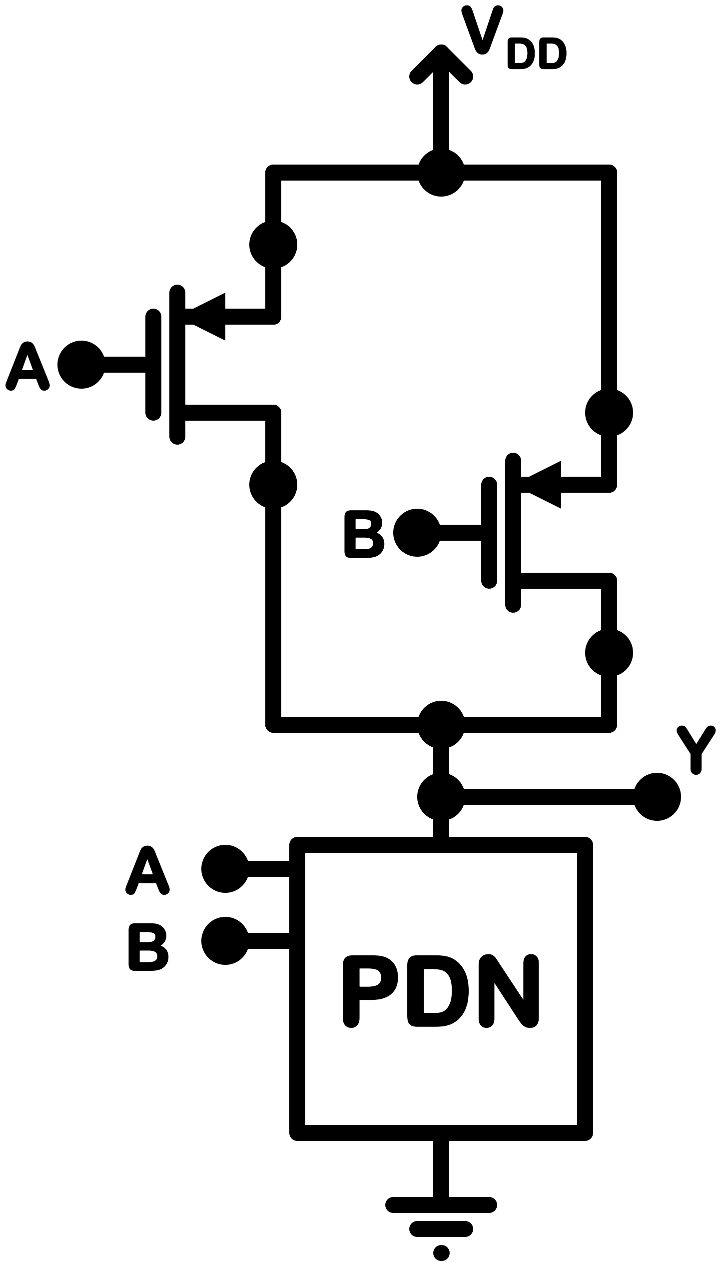


Two Complementary Networks

CMOS Inverter:

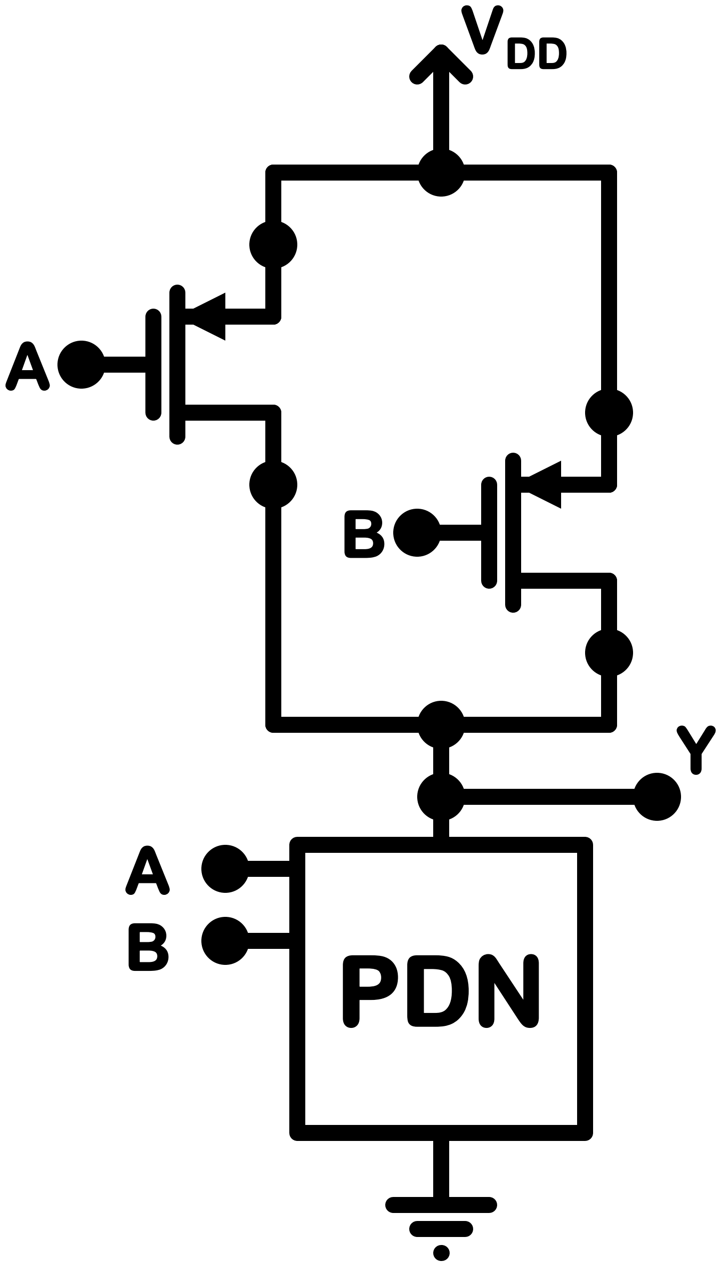
- Networks must be complementary:
  When PUN is conducting, PDN is open.
  When PDN is conducting, PUN is open.
- Both open would leave Y floating.
- Both conducting would dissipate more power and leave Y in transition region.

Combinational Logic Design: Parallel PMOS PUN



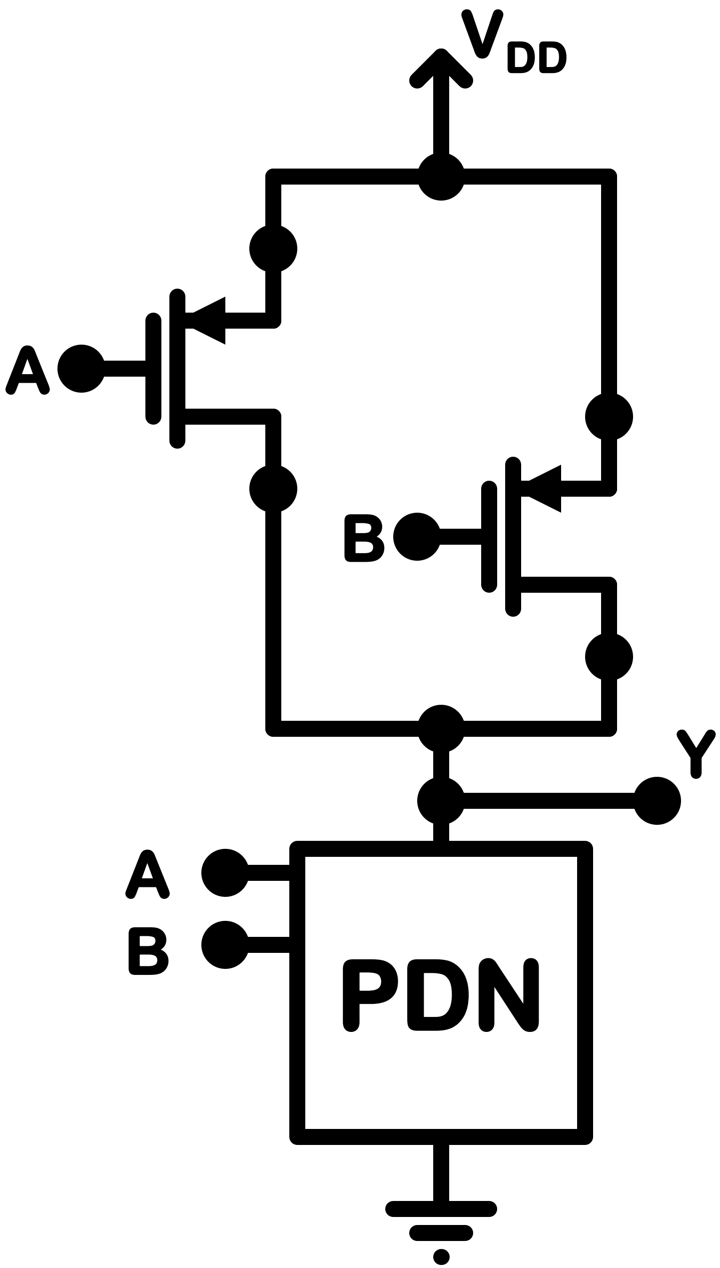
A	B	r_{SDA}	r_{SDB}	r_{PUN}	r_{PDN}	Y
0	0					
0	1					
1	0					
1	1					

Combinational Logic Design: Parallel PMOS PUN



A	B	r_{SDA}	r_{SDB}	r_{PUN}	r_{PDN}	Y
0	0	r_{SD}	r_{SD}	$r_{SD}/2$	o.c.	1
0	1	r_{SD}	o.c.	r_{SD}	o.c.	1
1	0	o.c.	r_{SD}	r_{SD}	o.c.	1
1	1	o.c.	o.c.	o.c.	r_{PDN}	0

Combinational Logic Design: Parallel PMOS PUN



A	B	r_{SDA}	r_{SDB}	r_{PUN}	r_{PDN}	Y
0	0	r_{SD}	r_{SD}	$r_{SD}/2$	o.c.	1
0	1	r_{SD}	o.c.	r_{SD}	o.c.	1
1	0	o.c.	r_{SD}	r_{SD}	o.c.	1
1	1	o.c.	o.c.	o.c.	r_{PDN}	0

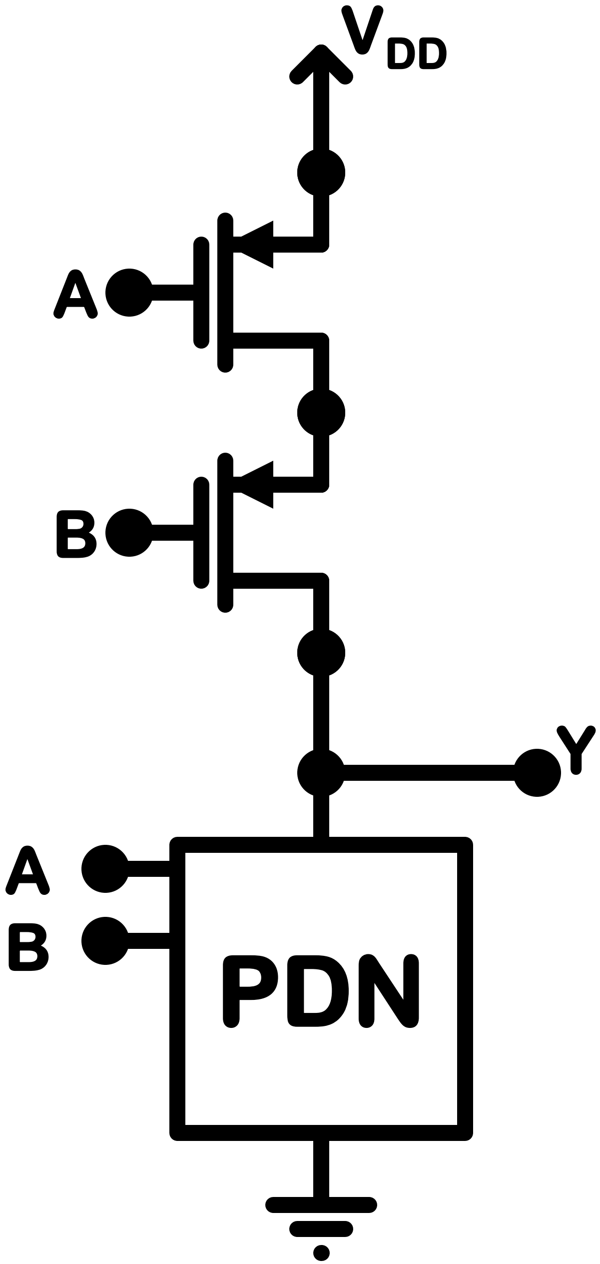
This is a NAND Gate

$$Y = \overline{A \cdot B}$$

But we like to use

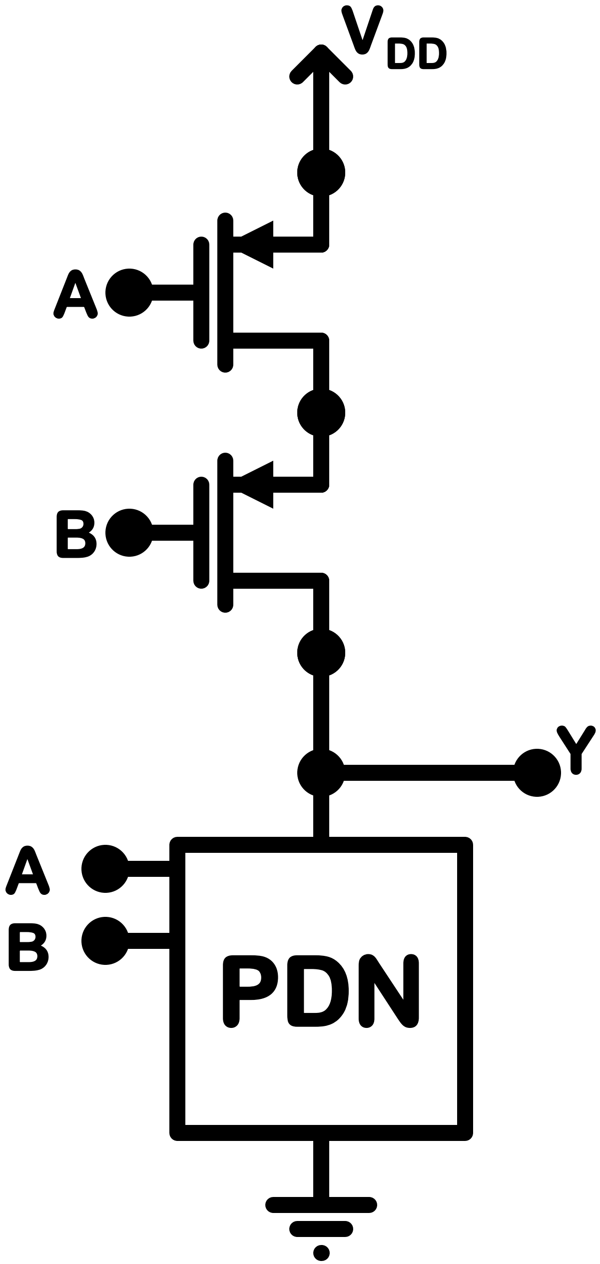
$$Y = \overline{A} + \overline{B}$$

Combinational Logic Design: Series PMOS PUN



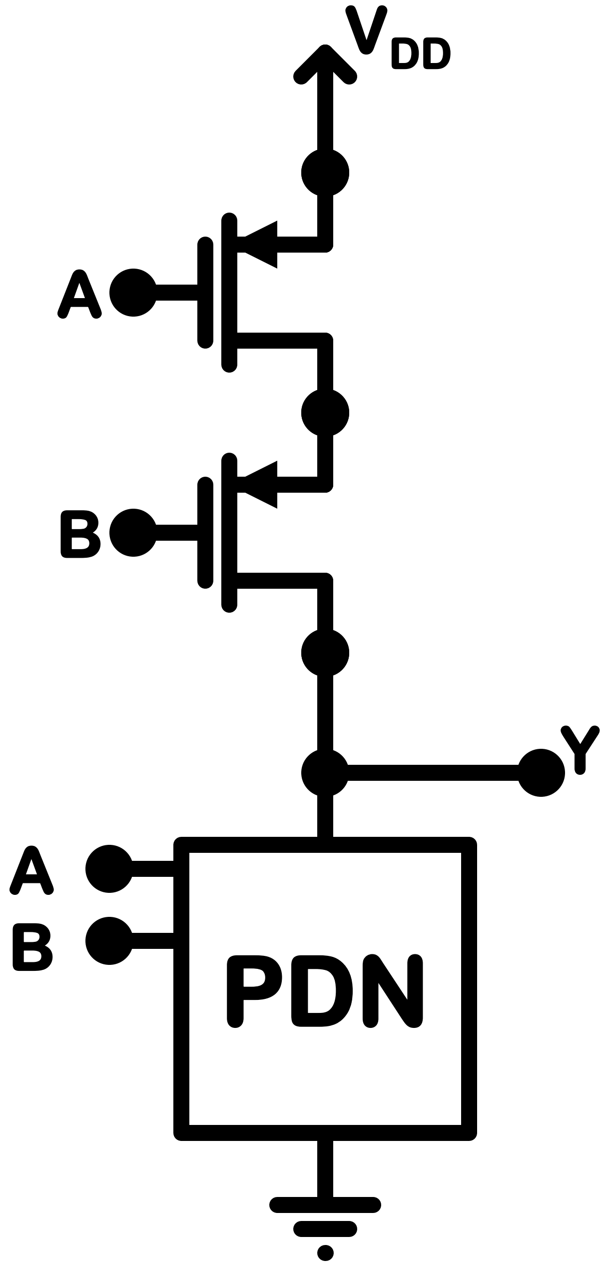
A	B	r_{SDA}	r_{SDB}	r_{PUN}	r_{PDN}	Y
0	0					
0	1					
1	0					
1	1					

Combinational Logic Design: Series PMOS PUN



A	B	r_{SDA}	r_{SDB}	r_{PUN}	r_{PDN}	Y
0	0	r_{SD}	r_{SD}	$2r_{SD}$	o.c.	1
0	1	r_{SD}	o.c.	o.c.	r_{PDN}	0
1	0	o.c.	r_{SD}	o.c.	r_{PDN}	0
1	1	o.c.	o.c.	o.c.	r_{PDN}	0

Combinational Logic Design: Series PMOS PUN



A	B	r_{SDA}	r_{SDB}	r_{PUN}	r_{PDN}	Y
0	0	r_{SD}	r_{SD}	$2r_{SD}$	o.c.	1
0	1	r_{SD}	o.c.	o.c.	r_{PDN}	0
1	0	o.c.	r_{SD}	o.c.	r_{PDN}	0
1	1	o.c.	o.c.	o.c.	r_{PDN}	0

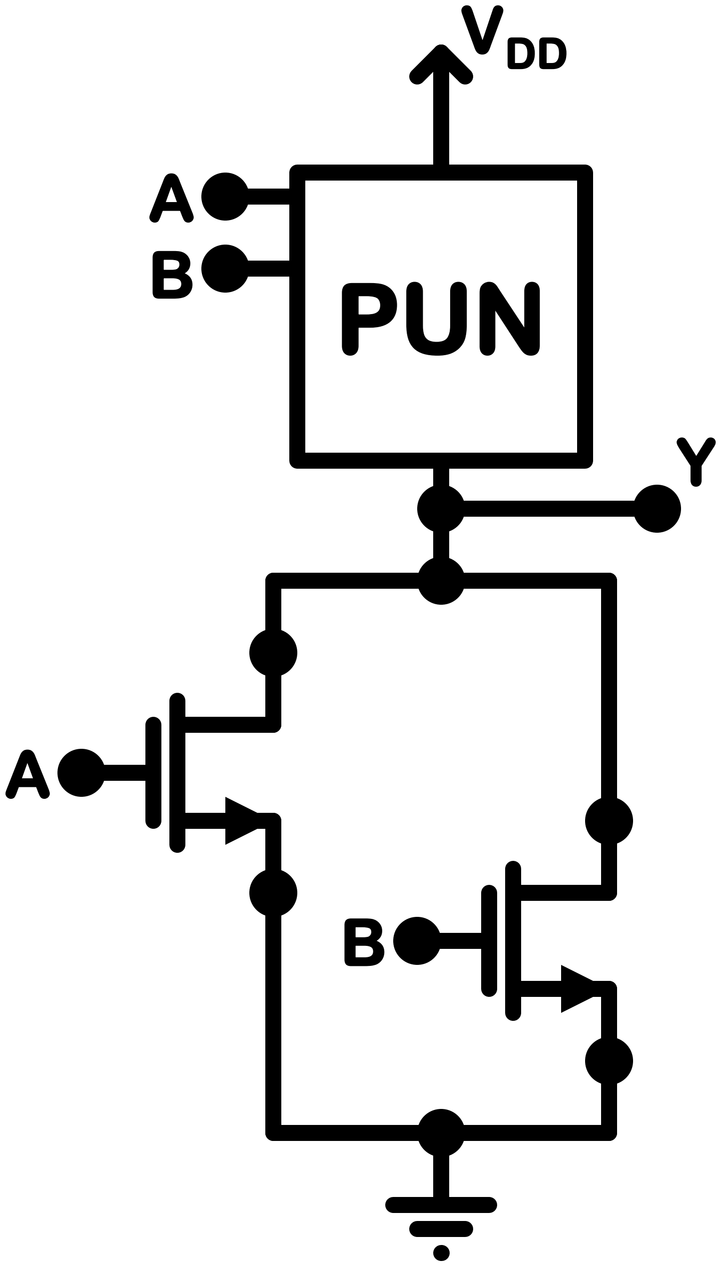
This is a NOR Gate

$$Y = \overline{A + B}$$

But we like to use

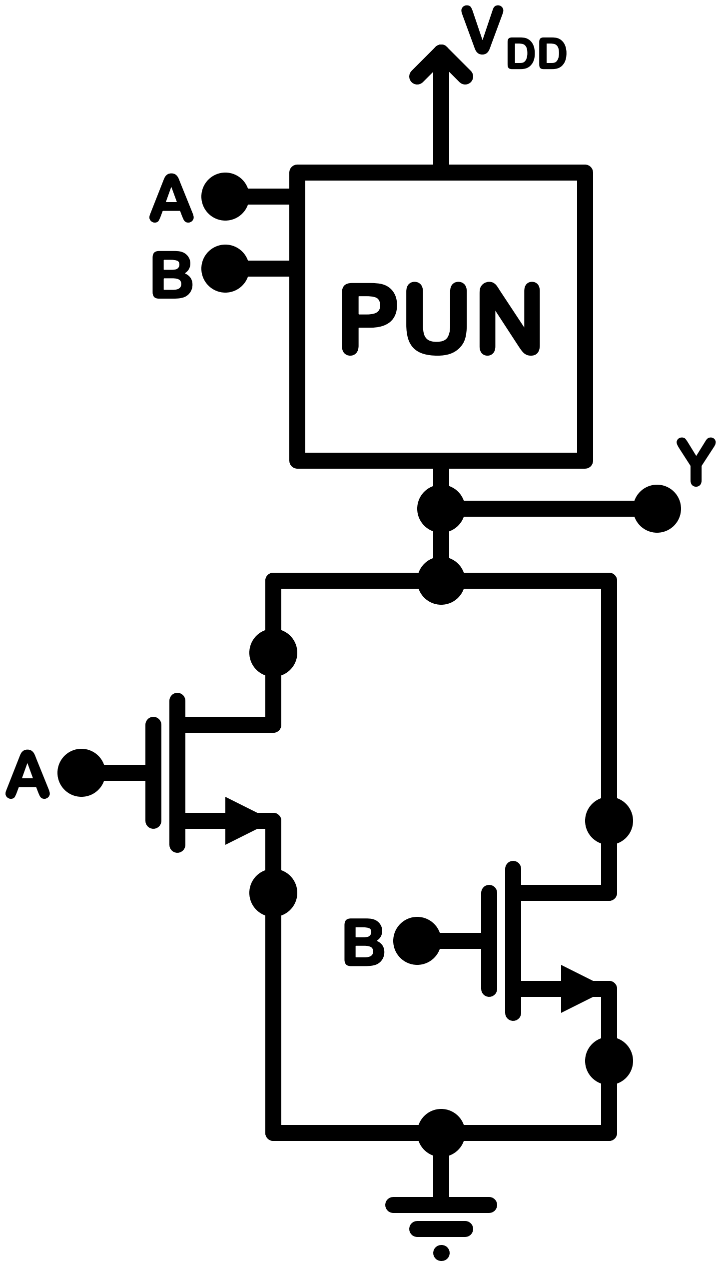
$$Y = \overline{A} \cdot \overline{B}$$

Combinational Logic Design: Parallel NMOS PDN



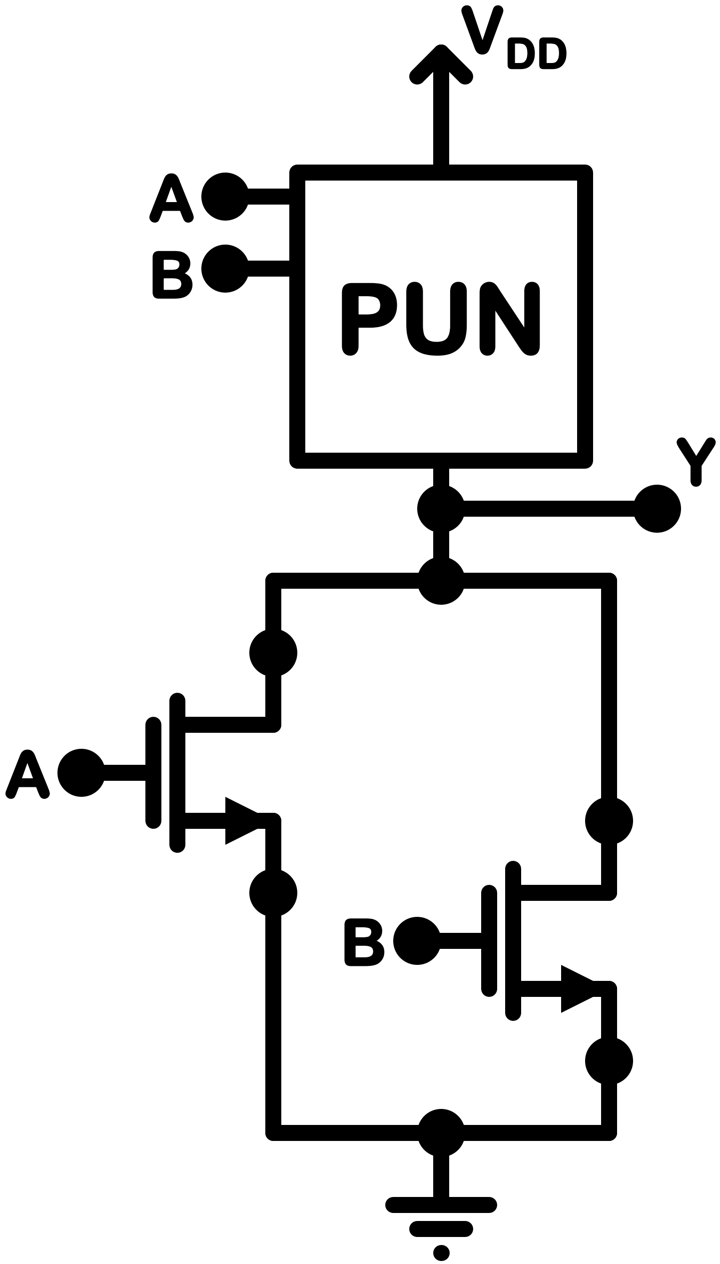
A	B	r_{DSA}	r_{DSB}	r_{PDN}	r_{PUN}	Y
0	0					
0	1					
1	0					
1	1					

Combinational Logic Design: Parallel NMOS PDN



A	B	r_{DSA}	r_{DSB}	r_{PDN}	r_{PUN}	Y
0	0	o.c.	o.c.	o.c.	r_{PUN}	1
0	1	o.c.	r_{DS}	r_{DS}	o.c.	0
1	0	r_{DS}	o.c.	r_{DS}	o.c.	0
1	1	r_{DS}	r_{DS}	$r_{DS}/2$	o.c.	0

Combinational Logic Design: Parallel NMOS PDN



A	B	r_{DSA}	r_{DSB}	r_{PDN}	r_{PUN}	Y
0	0	o.c.	o.c.	o.c.	r_{PUN}	1
0	1	o.c.	r_{DS}	r_{DS}	o.c.	0
1	0	r_{DS}	o.c.	r_{DS}	o.c.	0
1	1	r_{DS}	r_{DS}	$r_{DS}/2$	o.c.	0

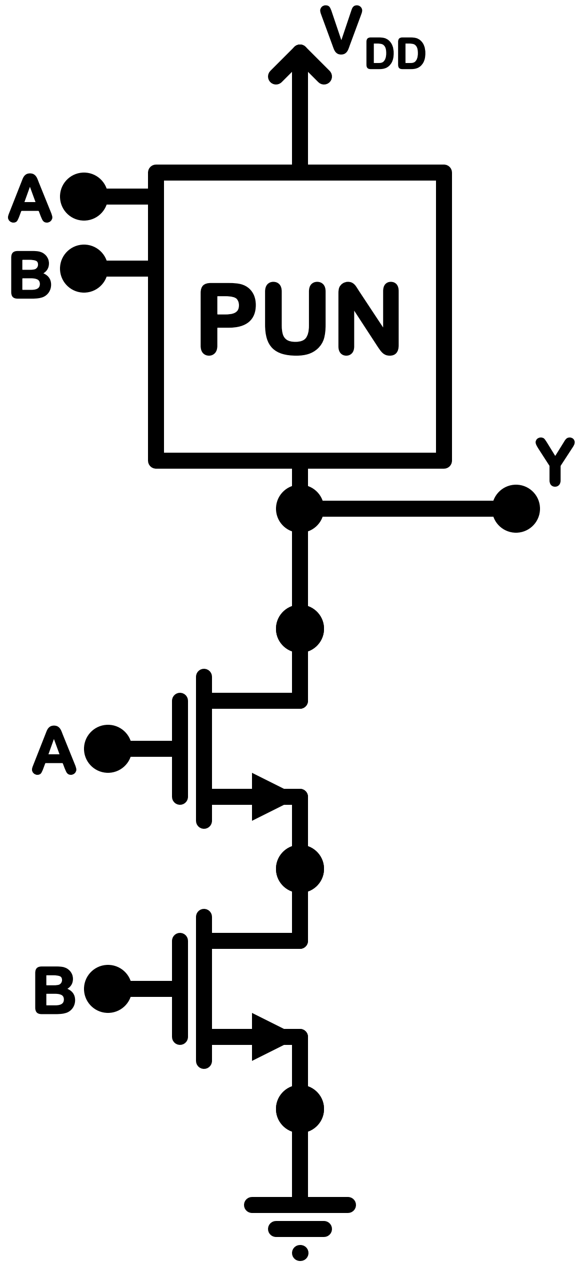
This is a NOR Gate

$$Y = \overline{A + B}$$

But we like to use

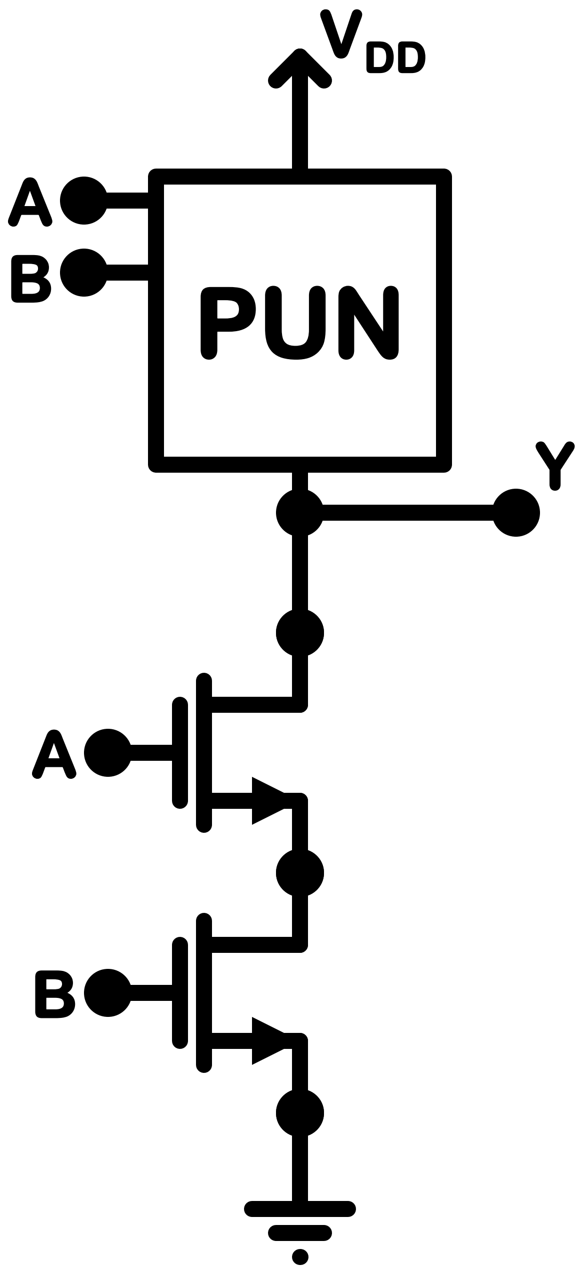
$$\overline{Y} = A + B$$

Combinational Logic Design: Series NMOS PDN



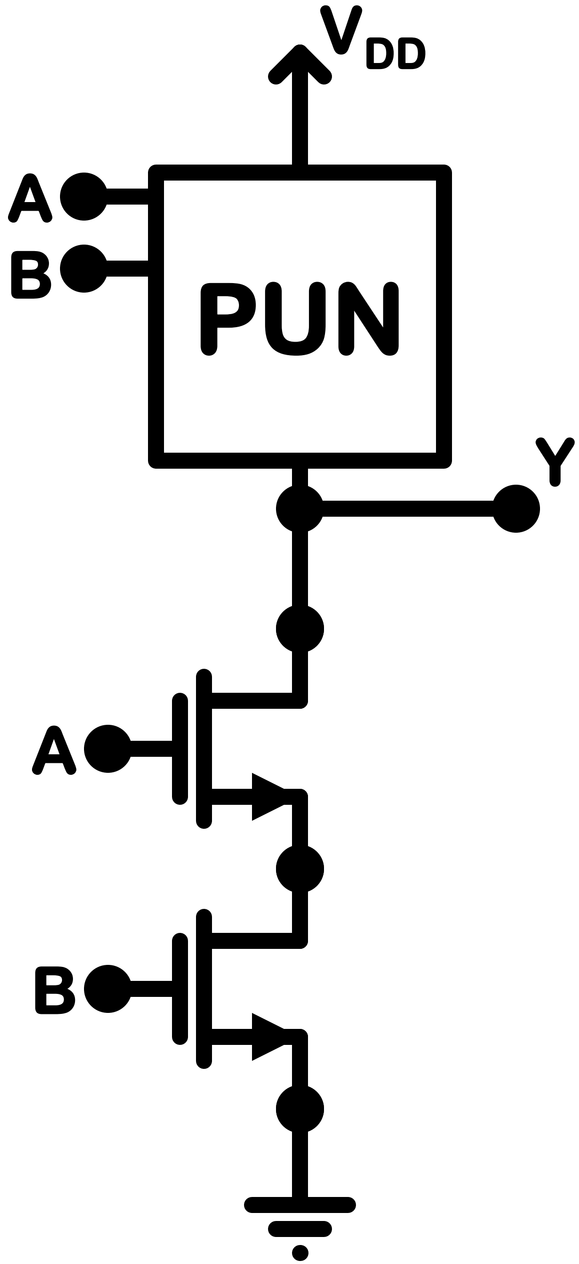
A	B	r_{DSA}	r_{DSB}	r_{PDN}	r_{PUN}	Y
0	0					
0	1					
1	0					
1	1					

Combinational Logic Design: Series NMOS PDN



A	B	r_{DSA}	r_{DSB}	r_{PDN}	r_{PUN}	Y
0	0	o.c.	o.c.	o.c.	r_{PUN}	1
0	1	o.c.	r_{DS}	o.c.	r_{PUN}	1
1	0	r_{DS}	o.c.	o.c.	r_{PUN}	1
1	1	r_{DS}	r_{DS}	$2r_{DS}$	o.c.	0

Combinational Logic Design: Series NMOS PDN



A	B	r_{DSA}	r_{DSB}	r_{PDN}	r_{PUN}	Y
0	0	o.c.	o.c.	o.c.	r_{PUN}	1
0	1	o.c.	r_{DS}	o.c.	r_{PUN}	1
1	0	r_{DS}	o.c.	o.c.	r_{PUN}	1
1	1	r_{DS}	r_{DS}	$2r_{DS}$	o.c.	0

This is a NAND Gate

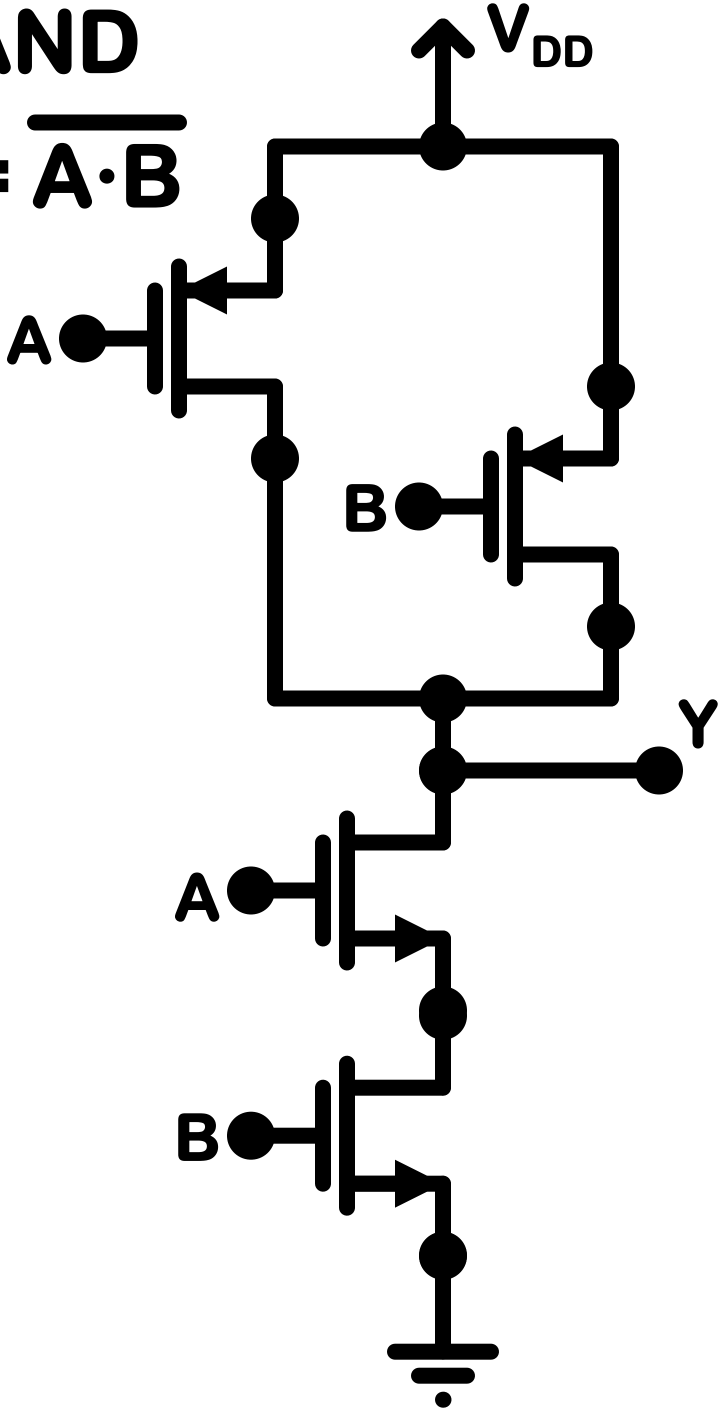
$$Y = \overline{A \cdot B}$$

But we like to use

$$\overline{Y} = A \cdot B$$

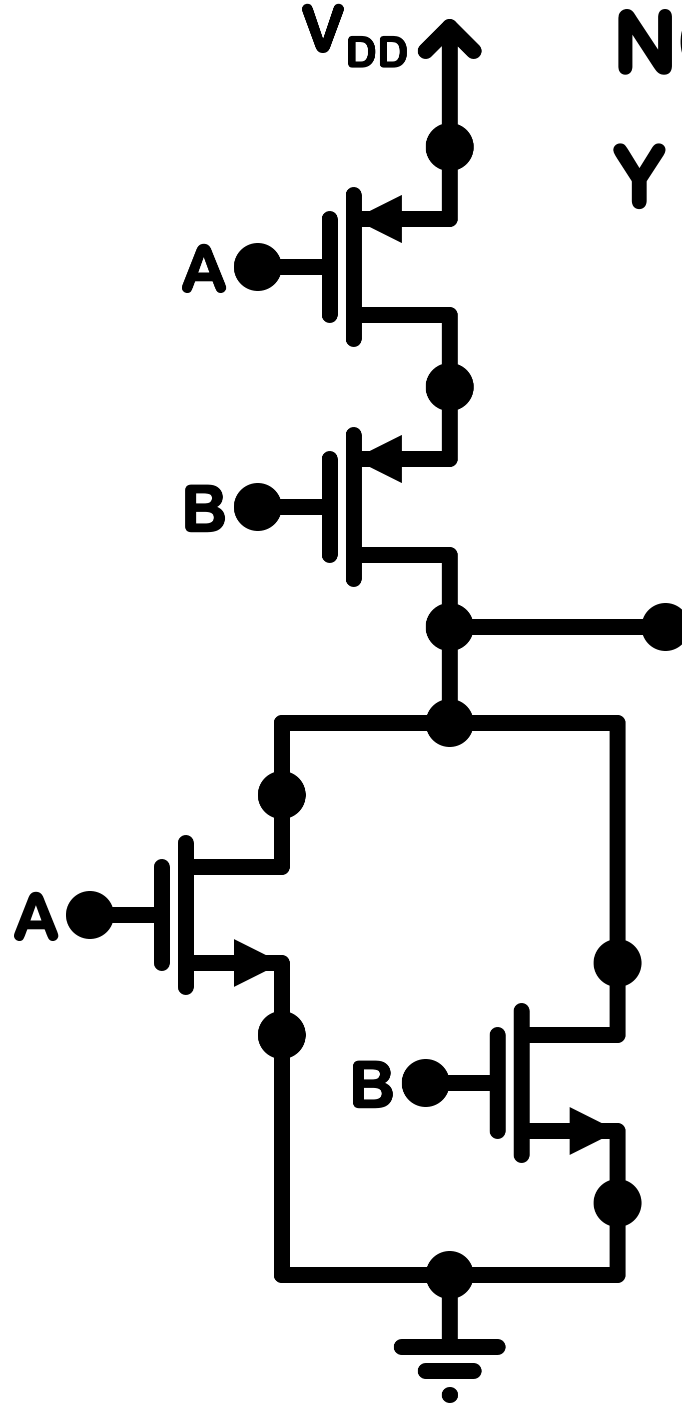
NAND

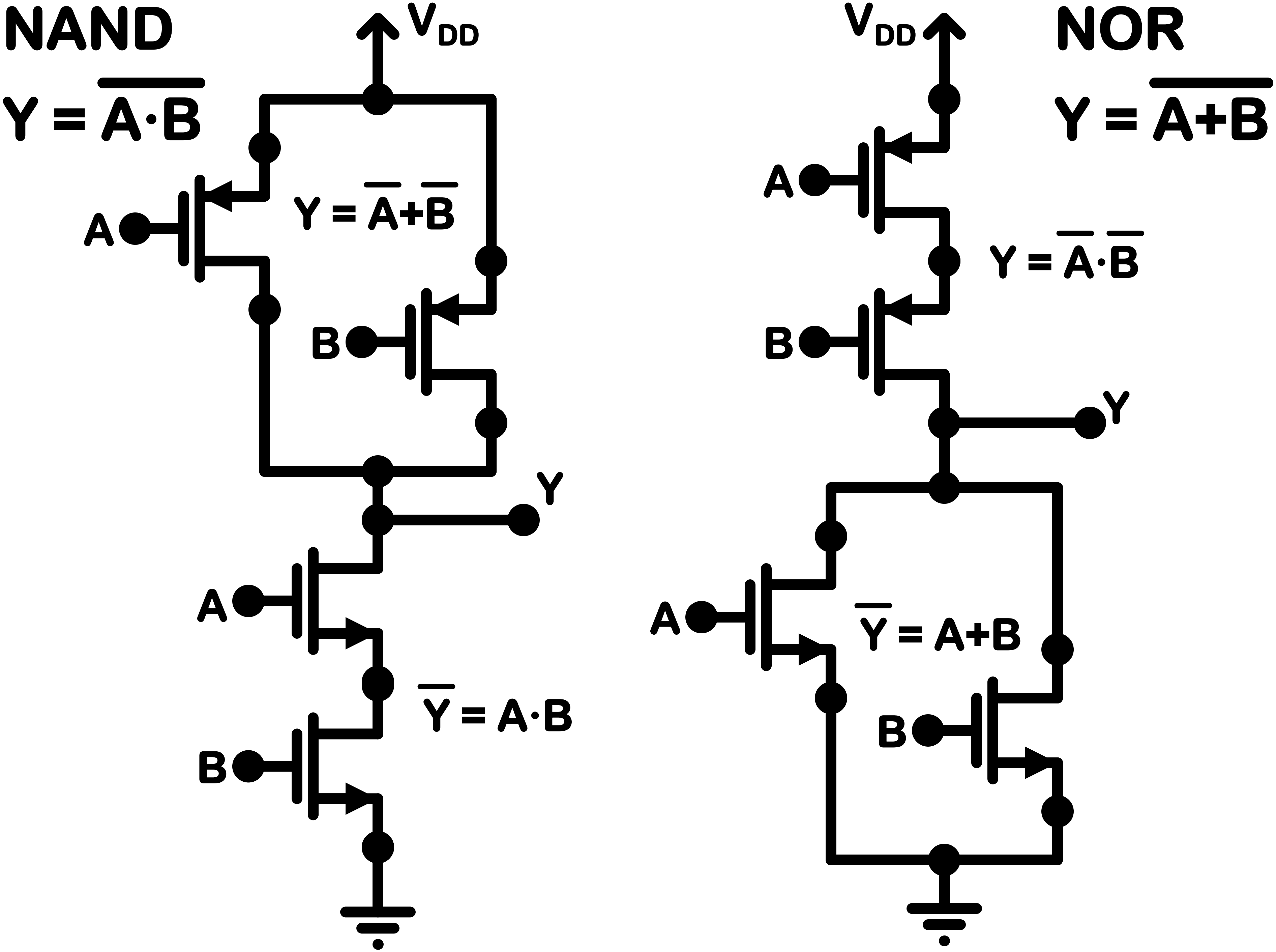
$Y = \overline{A \cdot B}$



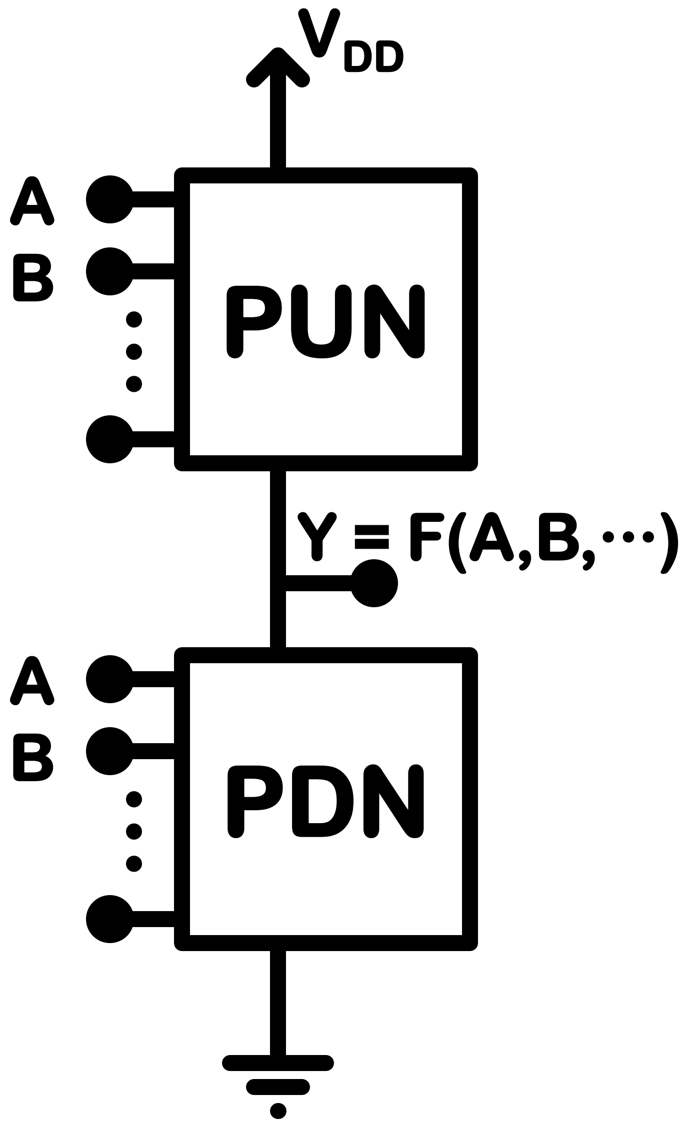
NOR

$Y = \overline{A + B}$




NAND
$Y = \overline{A \cdot B}$
V_{DD}
A
$Y = \overline{A} + \overline{B}$
B
Y
A
$\overline{Y} = A \cdot B$
B
V_{DD}
NOR
$Y = \overline{A + B}$
A
$Y = \overline{A} \cdot \overline{B}$
B
Y
A
$\overline{Y} = A + B$
B

Combinational Logic Design



Two Complementary Networks

Pull Up Network (PUN):

- Express Y in terms of inverted inputs.
- Constructed with PMOS devices.
- "ANDs" are serial connections.
- "ORs" are parallel connections.

Pull Down Network (PDN):

- Express inverted Y in terms inputs.
- Constructed with NMOS devices.
- "ANDs" are serial connections.
- "ORs" are parallel connections.

Combinational Logic Design: Examples

$$Y = \overline{A} \cdot (\overline{B} + \overline{C})$$

$$Y = \overline{A} \cdot \overline{B \cdot C + D}$$

Combinational Logic Design: Examples, find the function and PDN