Digital Logic … EECS140

Two Categories

Combinational

Sequential

Digital Logic … EECS140

Two Categories

Combinational

and, or, xor, …
*Output transitions with inputs.

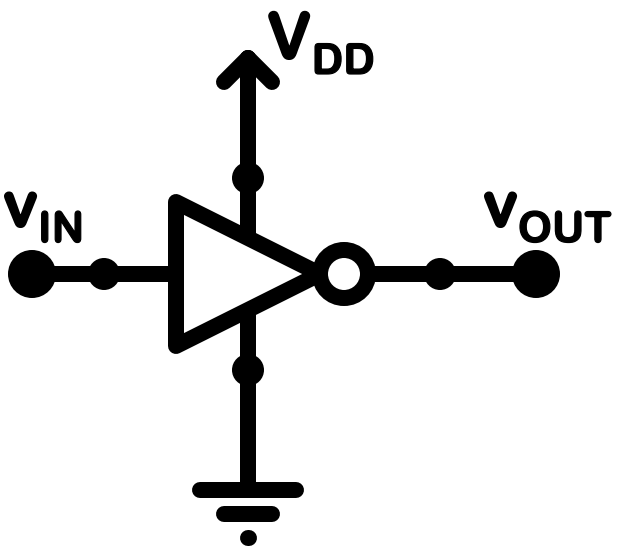
Sequential

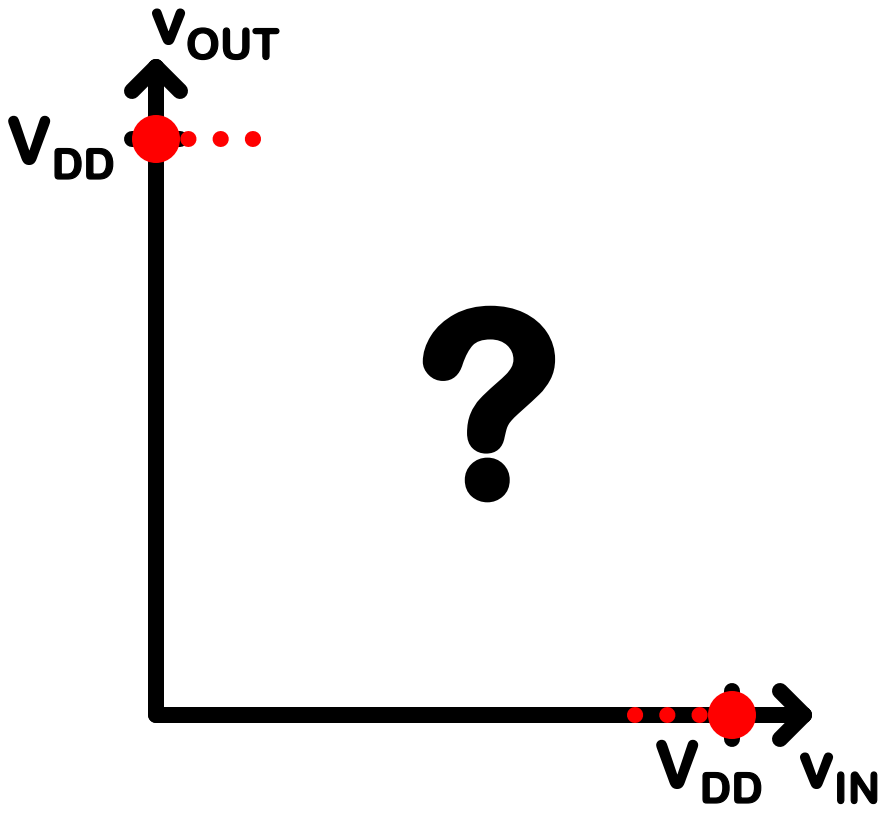
latch, FF, Memory
*Output Transitions with a clock or S/R.
*Holds its value.

Logic Design

Performance (speed, power, size)

The Ideal Inverter



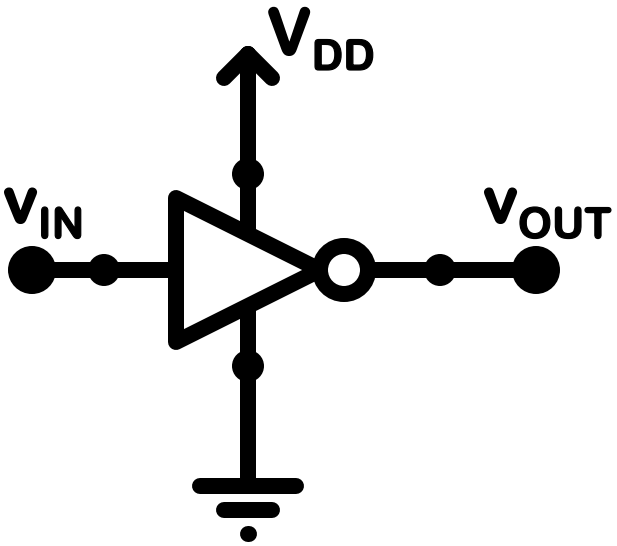


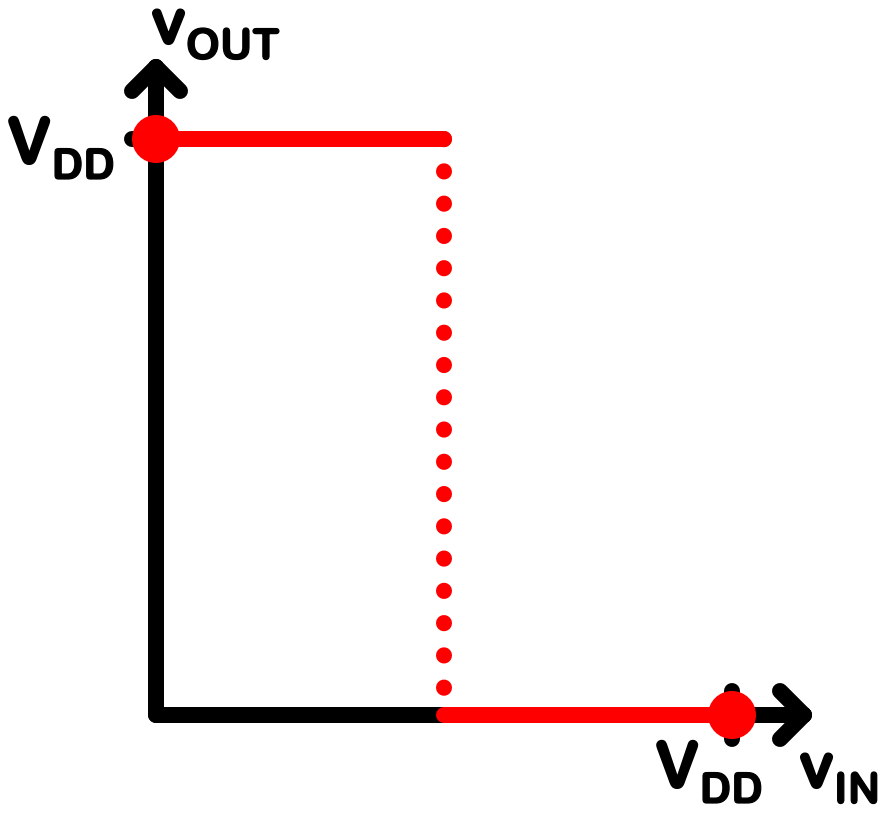
$v_{OUT} = V_{DD}$ at $v_{IN} = 0$

$v_{OUT} = 0$ at $v_{IN} = V_{DD}$

But what about between 0 and V_{DD}?

The Ideal Inverter



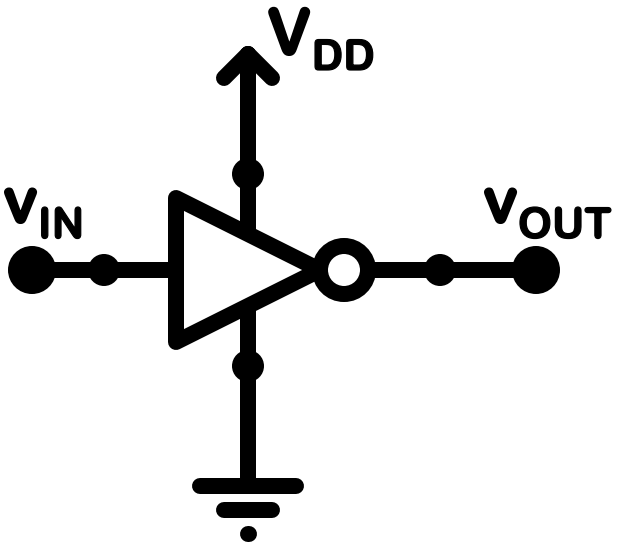


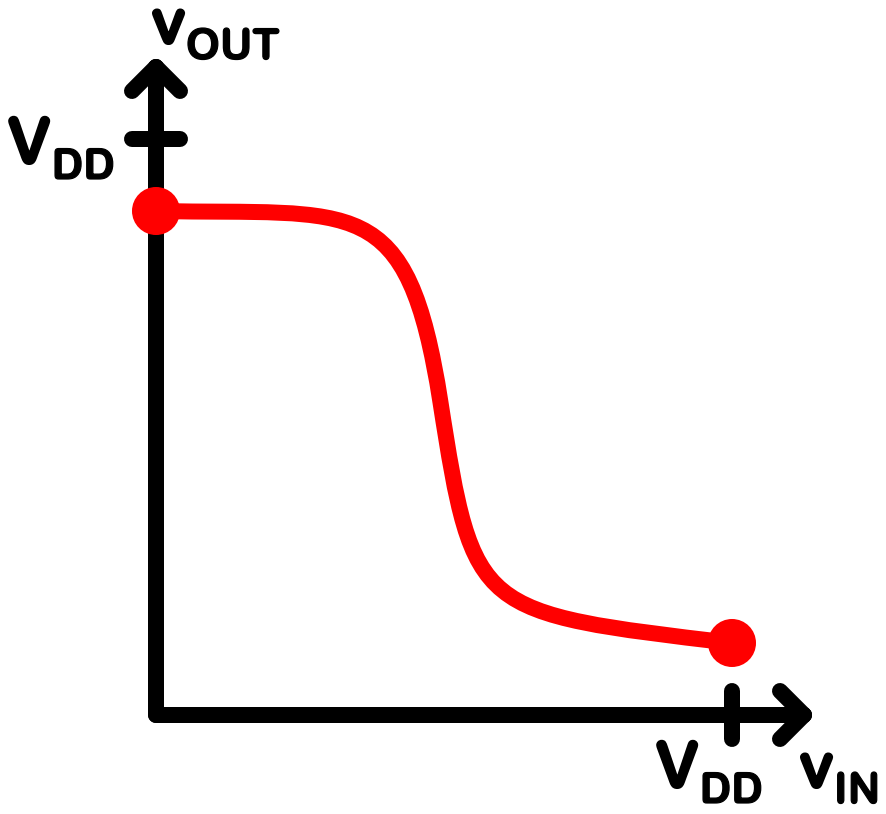
$v_{OUT} = V_{DD}$ for $v_{IN} < V_{DD}/2$

$v_{OUT} = 0$ for $v_{IN} > V_{DD}/2$

At $V_{DD}/2$ it is either V_{DD}, 0, or undefined.

A General Inverter

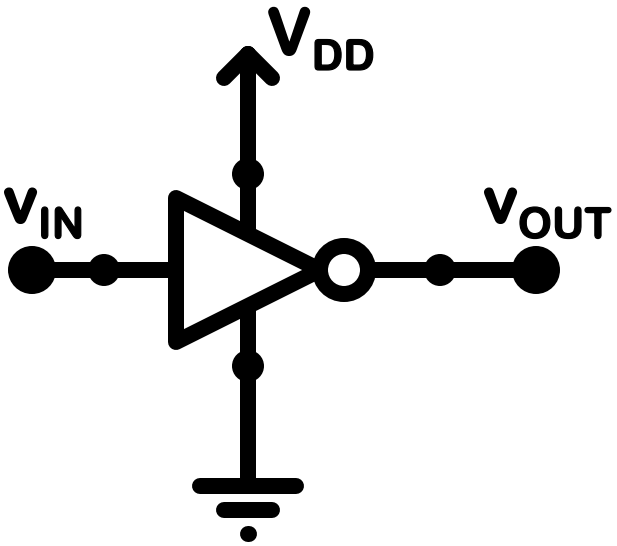


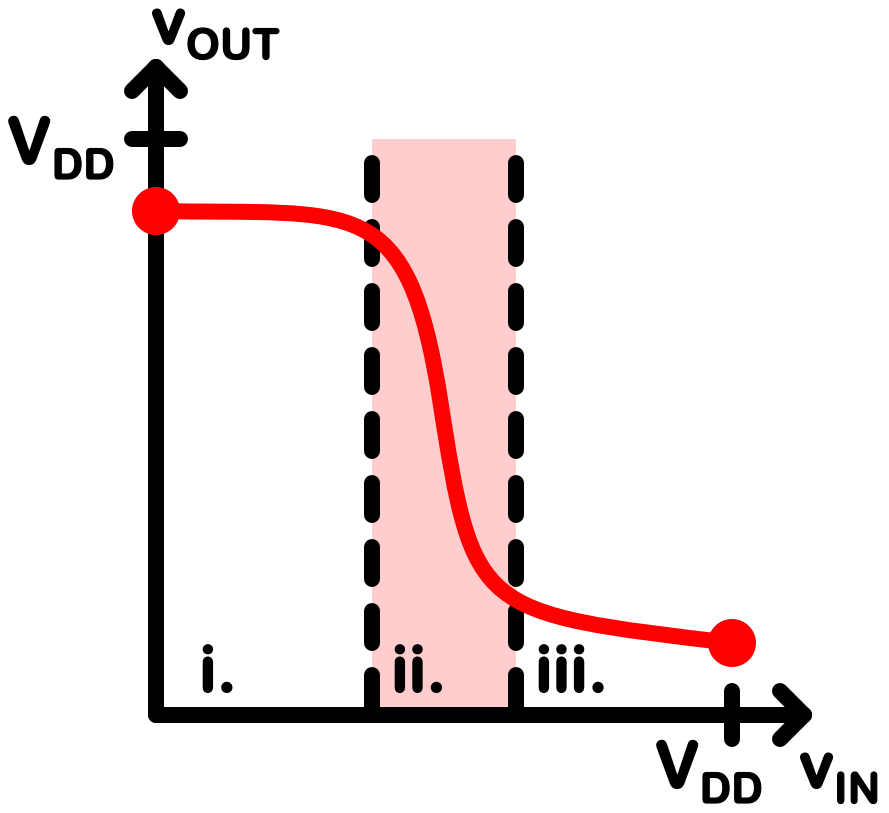


Observations:

- v_{OUT} doesn't necessarily equal V_{DD} at v_{IN}=0.
- v_{OUT} doesn't necessarily equal 0 at v_{IN}=V_{DD}.
- There is a transition region in between.
- The slope, $v_{OUT}'(v_{IN})$, is always negative.

A General Inverter





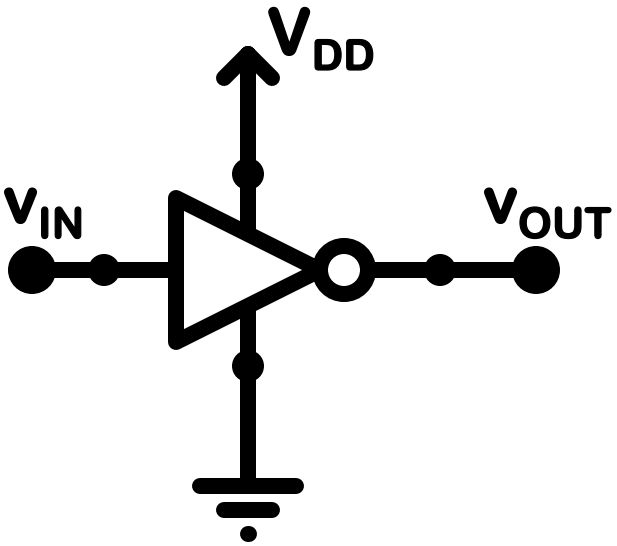
Regions:

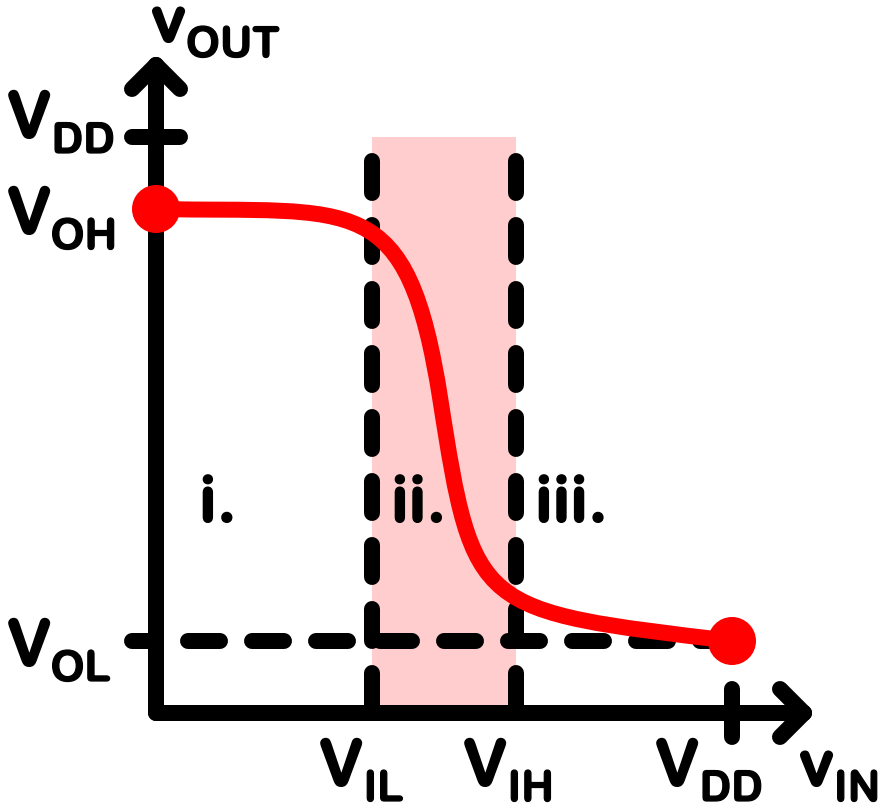
i. v_{IN} is LOW and v_{OUT} is HIGH.
$|v_{OUT}'(v_{IN})| < 1$, magnitude of slope is less than one.

ii. Transition Region (Stay out for Logic Applications).
$|v_{OUT}'(v_{IN})| > 1$, magnitude of slope is greater than one.

iii. v_{IN} is HIGH and v_{OUT} is LOW.
$|v_{OUT}'(v_{IN})| < 1$, magnitude of slope is less than one.

A General Inverter





Parameters

V_{OH}: Output High Voltage: $V_{OH} = v_{OUT}(0)$

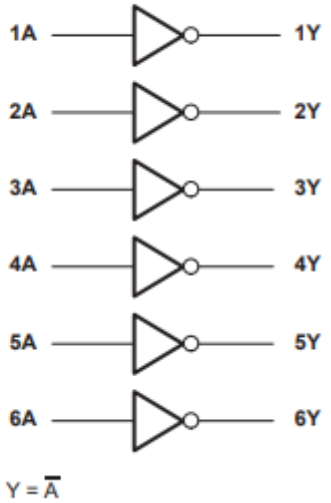
V_{OL}: Output Low Voltage: $V_{OL} = v_{OUT}(V_{DD})$

V_{IL}: Input Low Voltage: 1st point where $v_{OUT}'(v_{IN}) = -1$

V_{IH}: Input High Voltage: 2nd point where $v_{OUT}'(v_{IN}) = -1$

V_{IL} and V_{IH} are interpreted as values of v_{IN} that define the edges of the transition region, $v_{OUT}'(v_{IN})$ crosses -1.

logic diagram (positive logic)



$Y = \overline{A}$

recommended operating conditions (see Note 3)

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage							
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			SN5404			SN7404			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}¶	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			6	12		6	12	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			18	33		18	33	mA

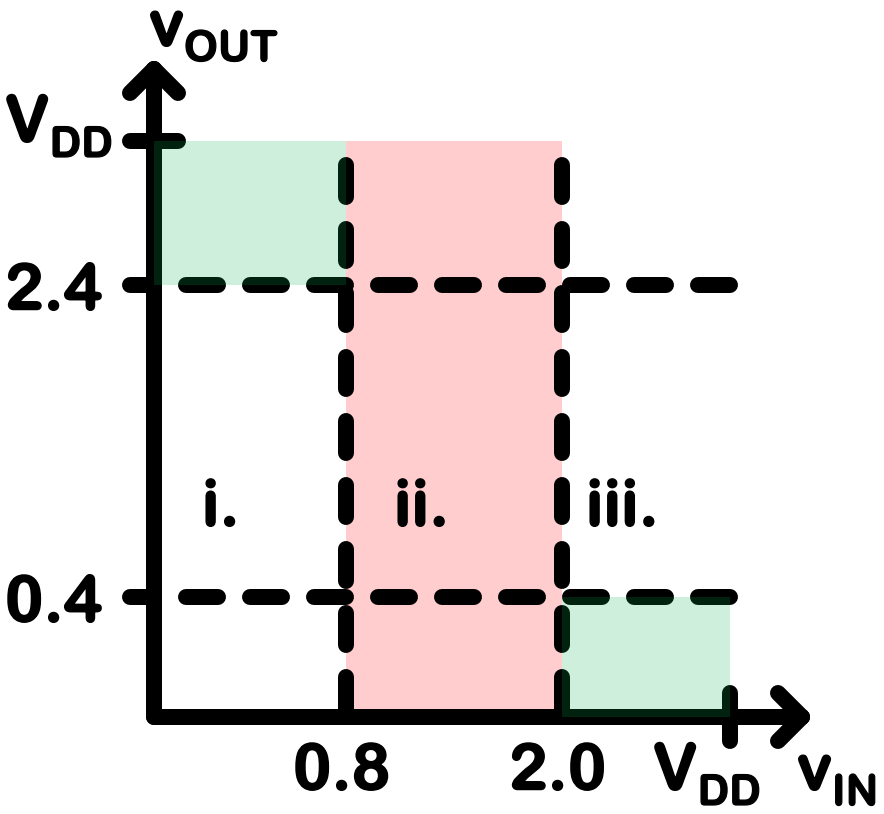
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

https://www.ti.com/lit/ds/symlink/sn74ahcu04-ep.pdf?ts=1679658099795

As long as the input is at least 2.0V, the input is registered high and the output will be low with a voltage that is at most 0.4V. ($v_{IN} > 2.0$, $v_{OUT} < 0.4$)

As long as the input is at most 0.8V, the input is registered low and the output will be high with a voltage that is at least 2.4V. ($v_{IN} < 0.8$, $v_{OUT} > 2.4$)

Why are these values important?

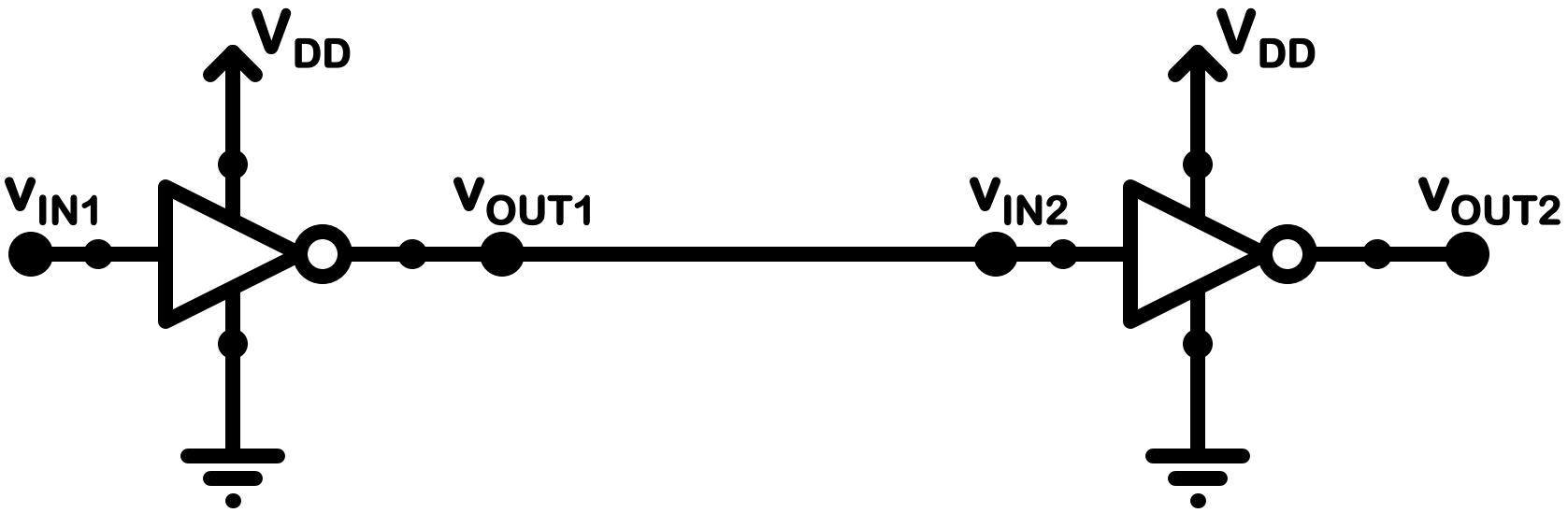


As long as the input is at least 2.0V, the input is registered high and the output will be low with a voltage that is at most 0.4V. ($v_{IN} > 2.0$, $v_{OUT} < 0.4$)

As long as the input is at most 0.8V, the input is registered low and the output will be high with a voltage that is at least 2.4V. ($v_{IN} < 0.8$, $v_{OUT} > 2.4$)

Why are these values important?
What if V_{OH} was actually 1.8V?

A General Inverter

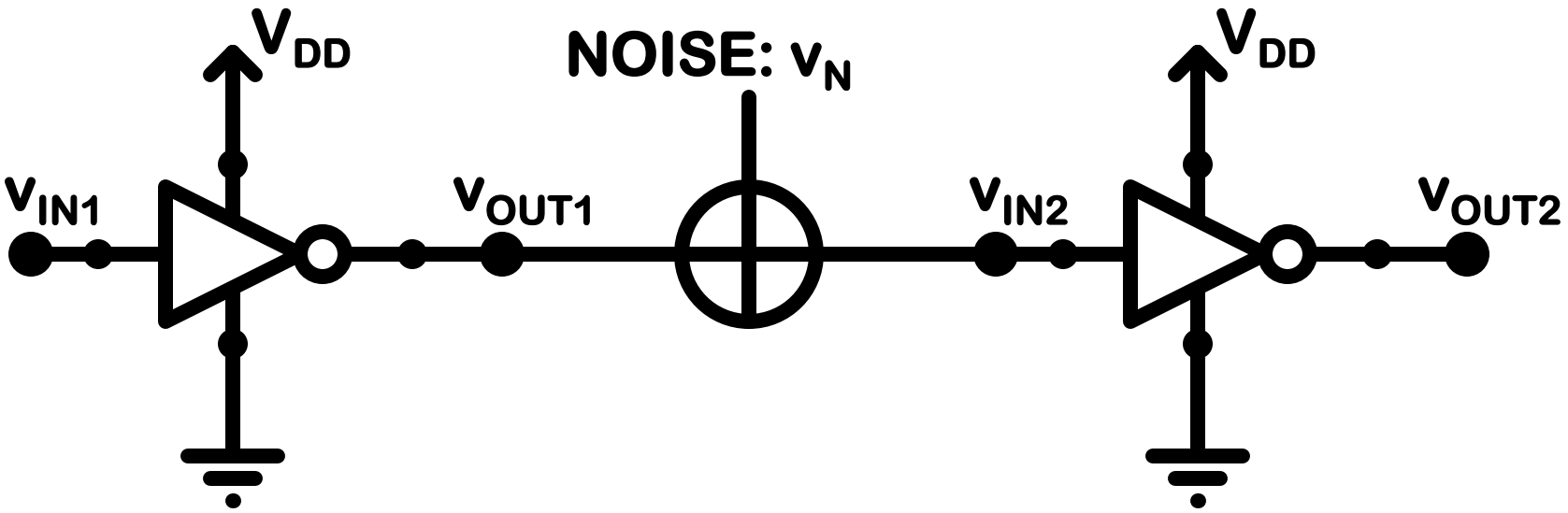


As long as the input is at least 2.0V, the input is registered high and the output will be low with a voltage that is at most 0.4V. ($v_{IN} > 2.0$, $v_{OUT} < 0.4$)

As long as the input is at most 0.8V, the input is registered low and the output will be high with a voltage that is at least 2.4V. ($v_{IN} < 0.8$, $v_{OUT} > 2.4$)

Why are these values important?
What if V_{OH} was actually 1.8V?

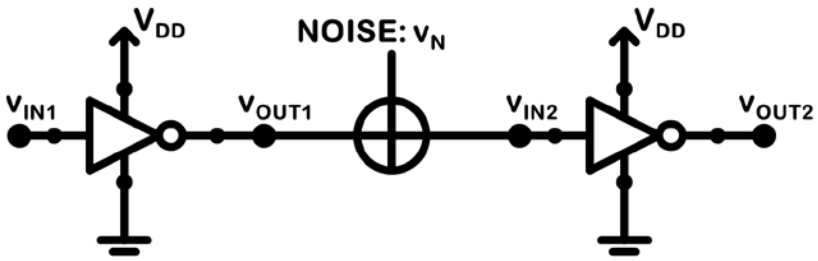
A General Inverter

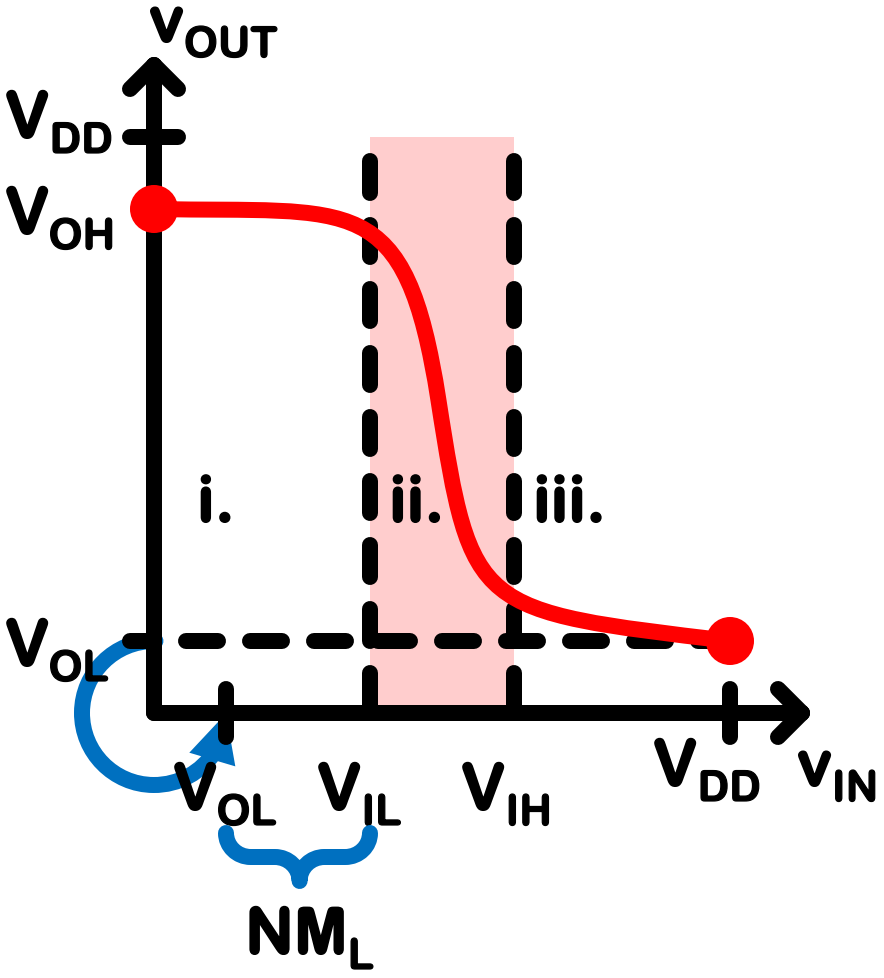


NOISE MARGIN: The maximum magnitude of noise that the circuit can tolerate to ensure v_{IN2} stays out of the transition region.

NM_L: when v_{IN1} is the ideal high input, V_{DD}.
NM_H: when v_{IN1} is the ideal low input, 0.
NM: The minimum value of NM_L or NM_H.

A General Inverter





NM_L:

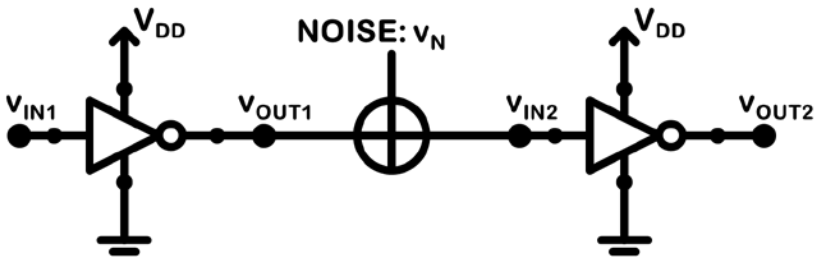
$v_{IN1} = V_{DD}$

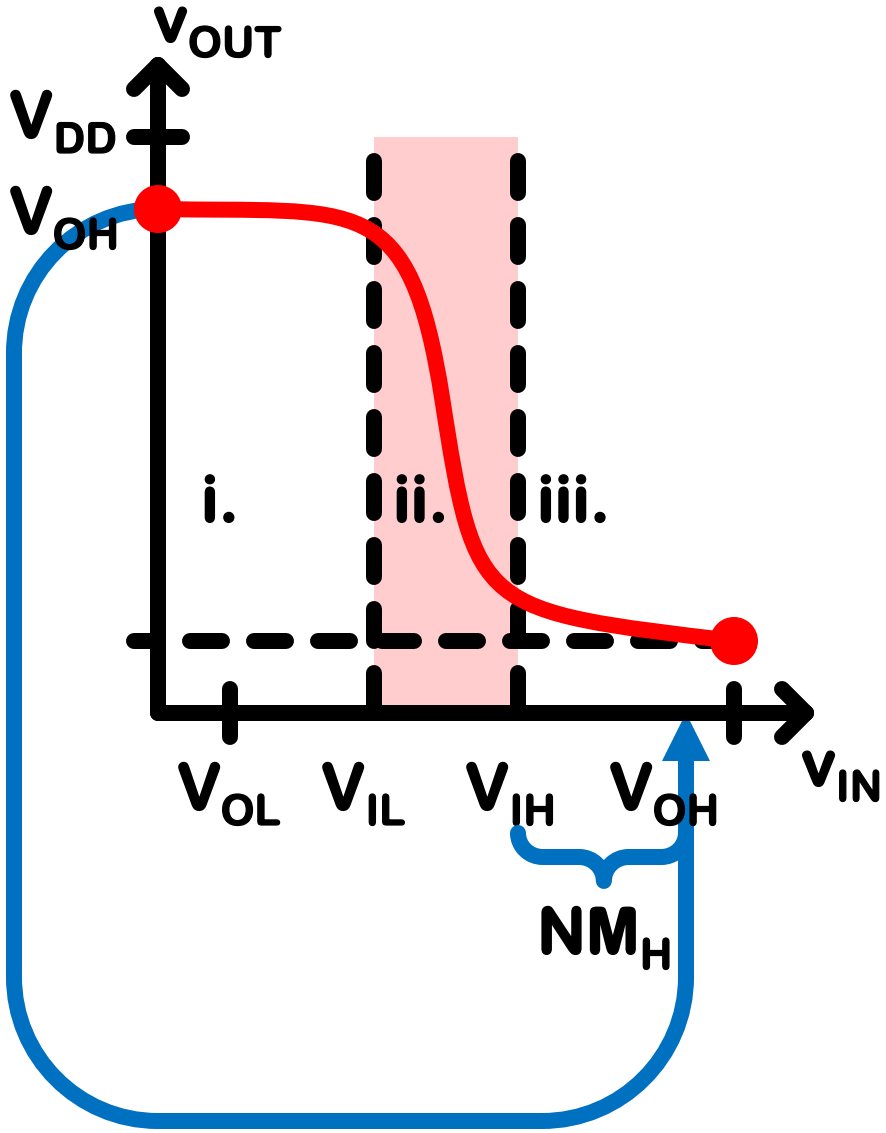
$v_{OUT1} = V_{OL}$

$v_{IN2} = V_{OL} + |v_N| < V_{IL}$

$v_N < V_{IL} - V_{OL} = NM_L$

A General Inverter





NM_H:

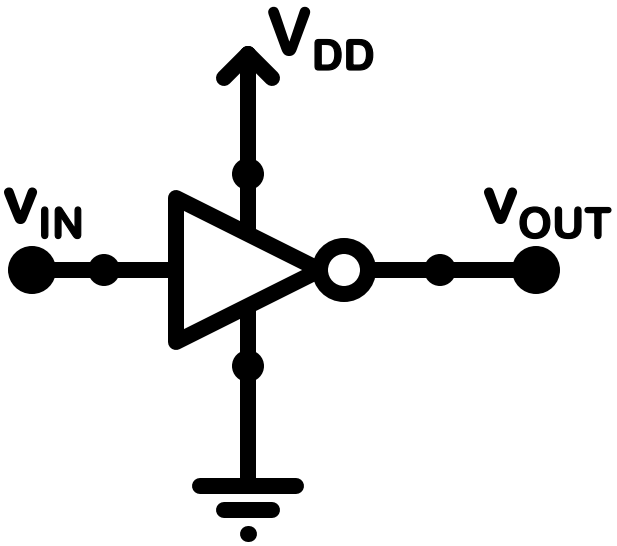
$v_{IN1} = 0$

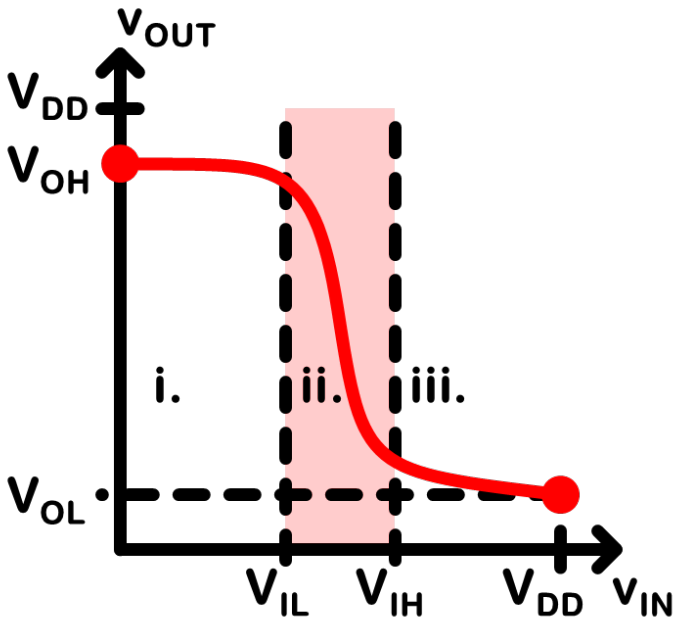
$v_{OUT1} = V_{OH}$

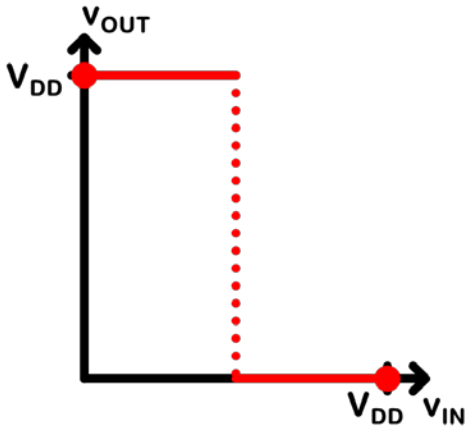
$v_{IN2} = V_{OH} - |v_N| > V_{IH}$

$v_N < V_{OH} - V_{IH} = NM_H$

A General Inverter





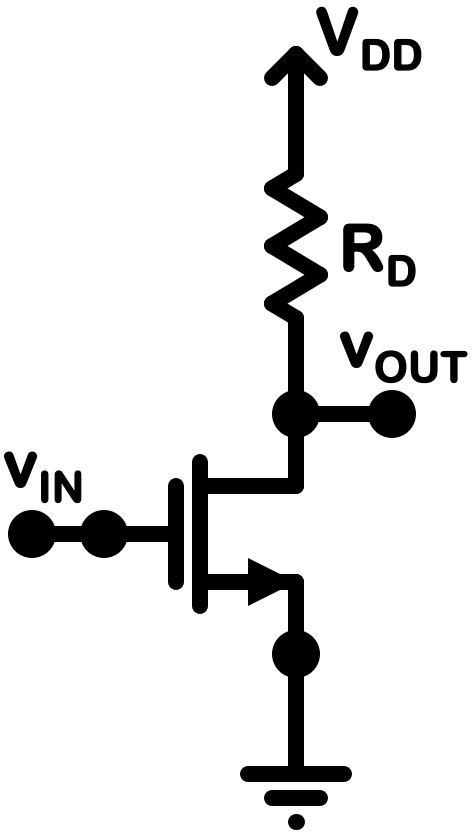


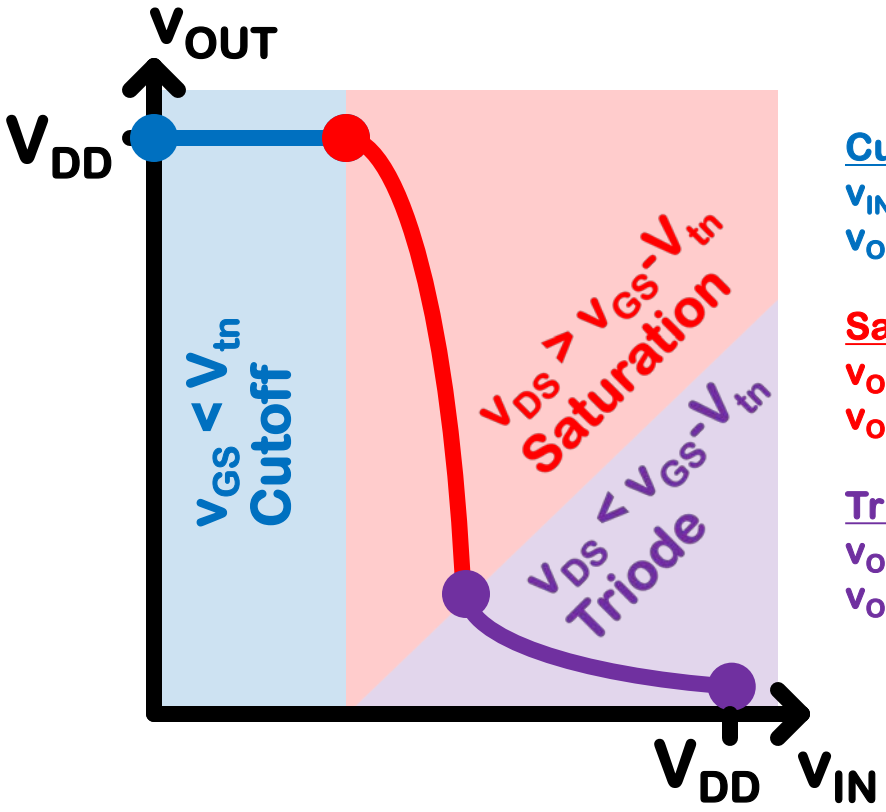
The Ideal Inverter achieves the maximum NM.

Parameters

V_{OH}:	Output High Voltage:	$V_{OH} = v_{OUT}(0)$
V_{OL}:	Output Low Voltage:	$V_{OL} = v_{OUT}(V_{DD})$
V_{IL}:	Input Low Voltage:	1st point where $v_{OUT}'(v_{IN}) = -1$
V_{IH}:	Input High Voltage:	2nd point where $v_{OUT}'(v_{IN}) = -1$
NM_L:	Noise Margin Low:	$NM_L = V_{IL} - V_{OL}$
NM_H:	Noise Margin High:	$NM_H = V_{OH} - V_{IH}$
NM:	Noise Margin:	$NM = \min(NM_L, NM_H)$

Implementation
NMOS Inverter





Cutoff

$v_{IN} < V_{tn}$

$v_{OUT} = V_{DD}$

Saturation

$v_{OUT} > v_{IN}-V_{tn}$

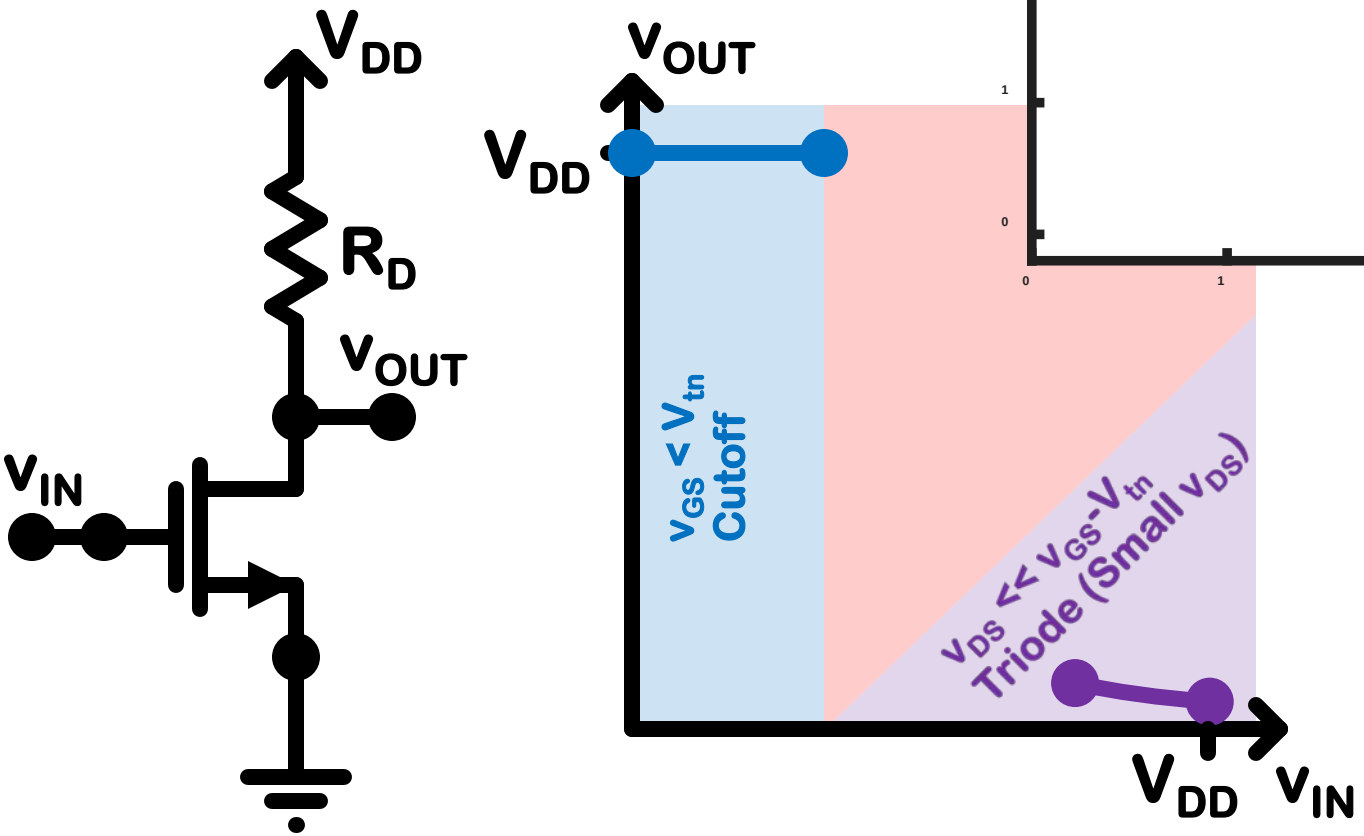
$v_{OUT} = V_{DD}-0.5R_Dk_n(v_{IN}-V_{tn})^2$

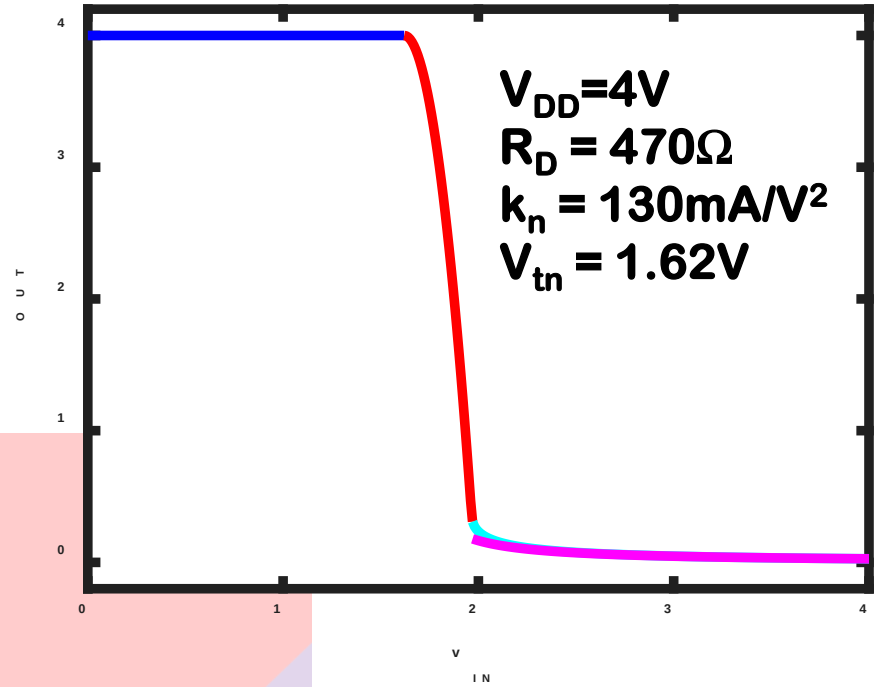
Triode (small v_{SD})

$v_{OUT} < v_{IN}-V_{tn}$

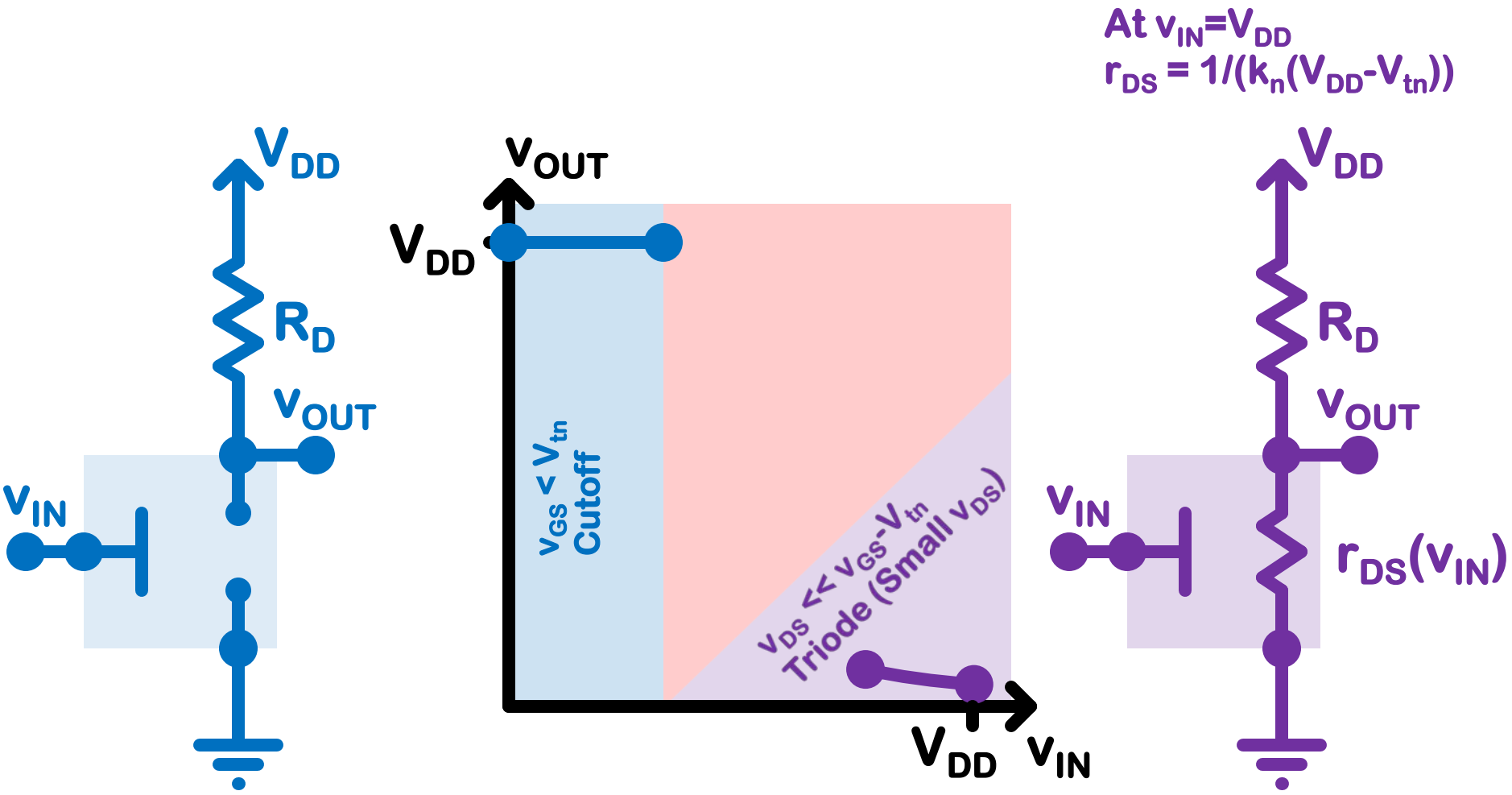
$v_{OUT} = V_{DD}/(1+R_Dk_n(v_{IN}-V_{tn}))$

NMOS Inverter



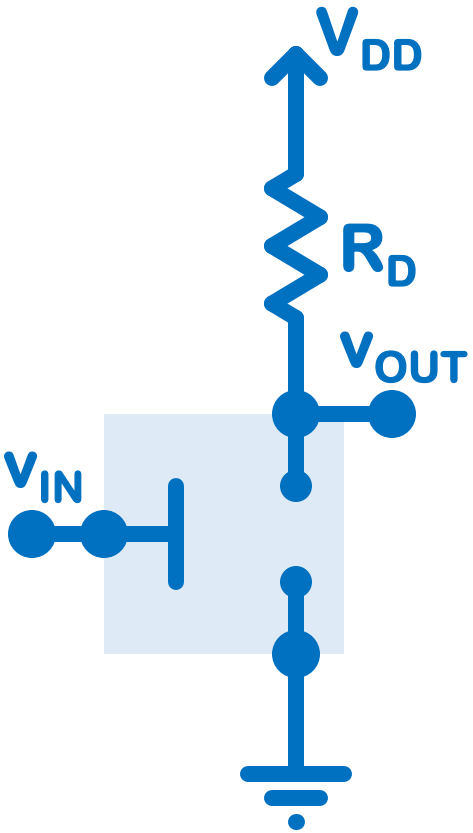


NMOS Inverter (models)

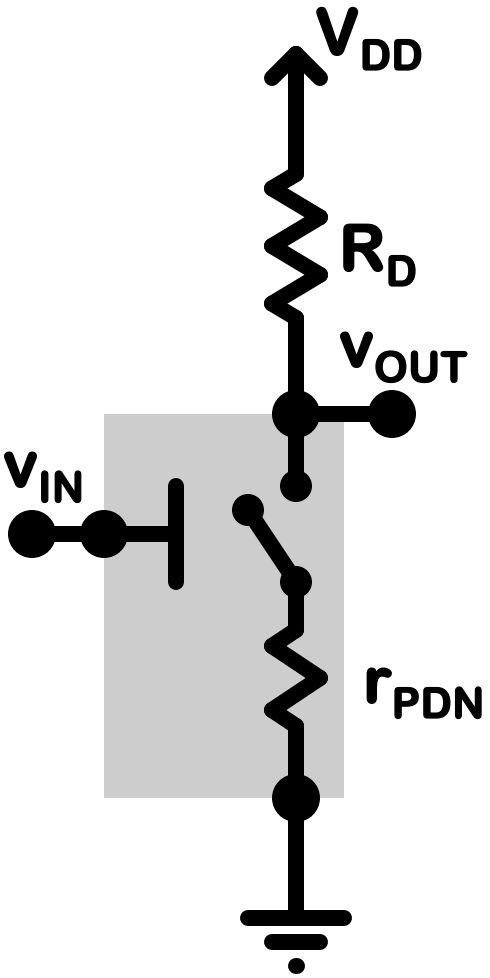


Basic Inverter
NMOS Inspired

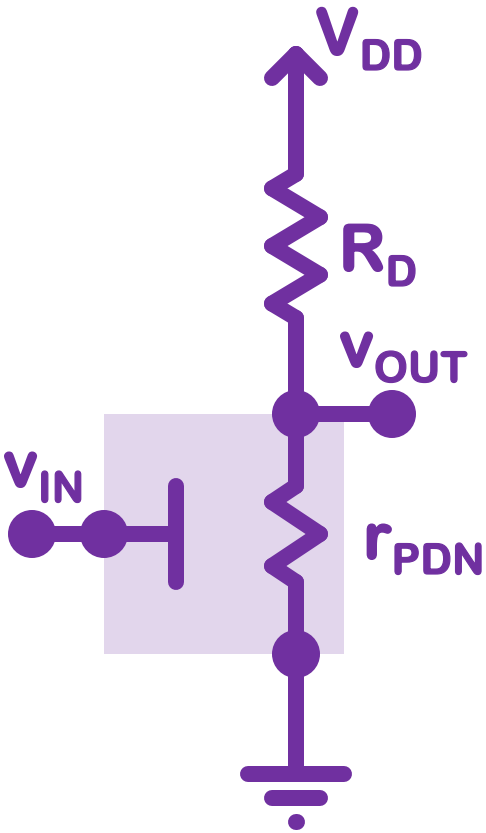
v_{IN} is LOW,
Switch is OPEN,
Not Conducting,
v_{OUT} is HIGH.



$P_D=0$



v_{IN} is HIGH,
Switch is CLOSED.
Conducting,
v_{OUT} is LOW.



$r_{PDN} = r_{DS} = 1/(k_n(v_{DD}-V_{tn}))$

$P_D=V_{DD}^2/(R_D+r_{PDN})$

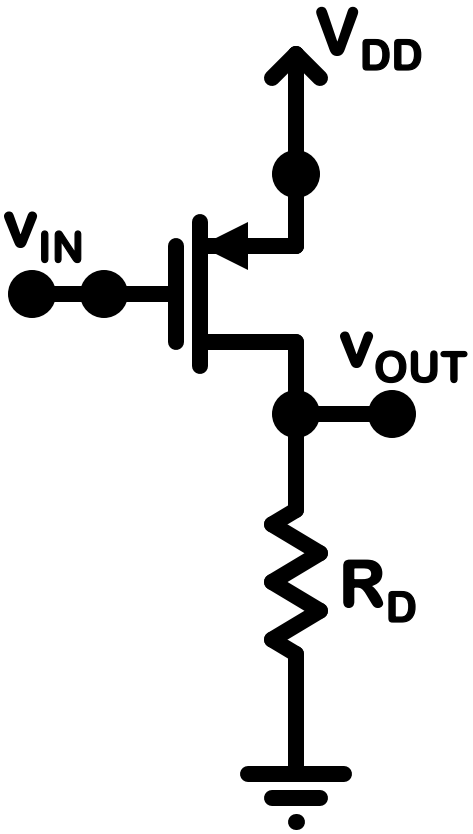
PMOS Inverter

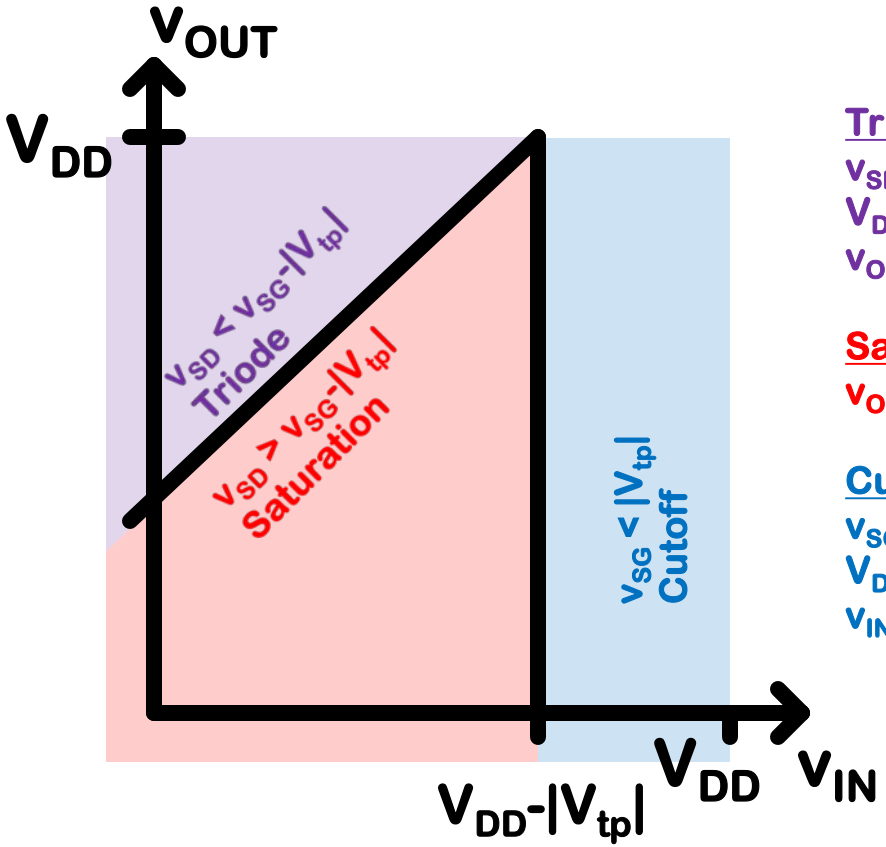
Notes:

$v_{IN} = V_{DD} - v_{SG}$

$v_{OUT} = V_{DD} - v_{SD} = R_D i_D$

As v_{IN} (or VDD – v_{SG}) increases from zero to V_{DD}.
Modes: triode, saturation, cutoff





Triode

$v_{SD} < v_{SG} - |V_{tp}|$

$V_{DD} - v_{OUT} < V_{DD} - v_{IN} - |V_{tp}|$

$v_{OUT} > v_{IN} + |V_{tp}|$

Saturation

$v_{OUT} < v_{IN} + |V_{tp}|$

Cutoff

$v_{SG} < |V_{tp}|$

$V_{DD} - v_{IN} < |V_{tp}|$

$v_{IN} > V_{DD} - |V_{tp}|$

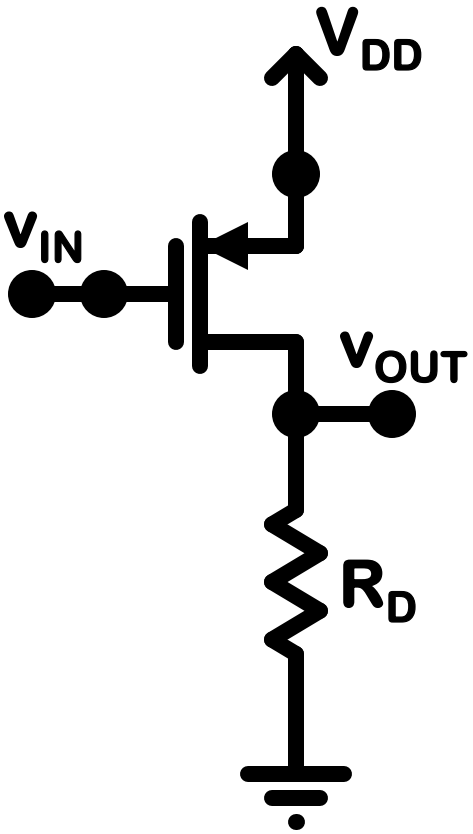
PMOS Inverter

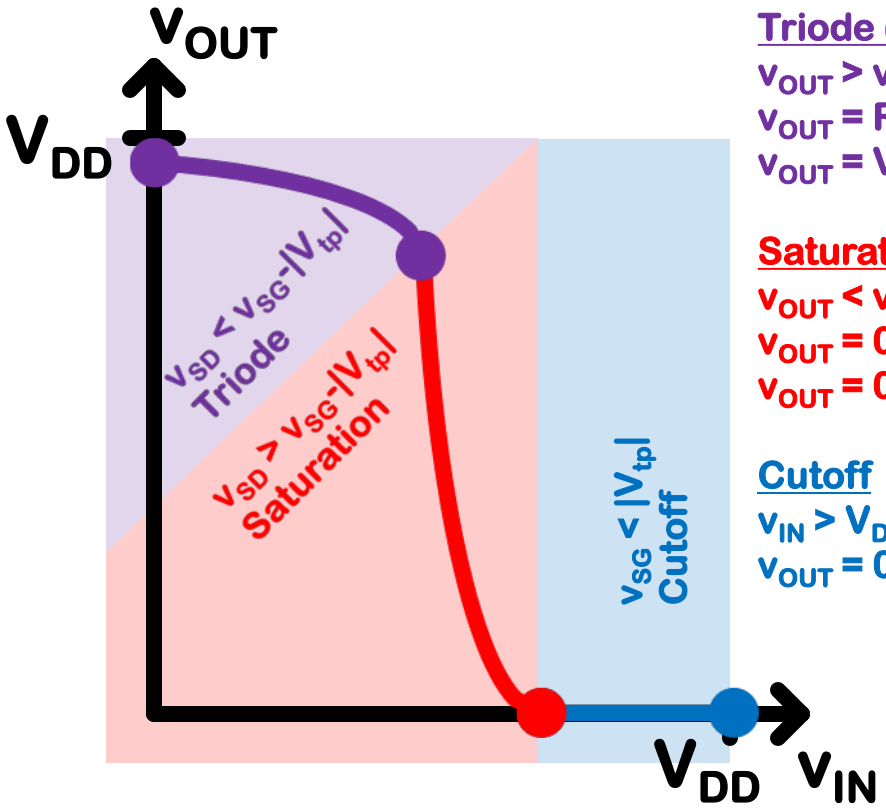
Notes:

$v_{IN} = V_{DD} - v_{SG}$

$v_{OUT} = V_{DD} - v_{SD} = R_D i_D$

As v_{IN} (or VDD – v_{SG}) increases from zero to V_{DD}.
Modes: triode, saturation, cutoff





Triode (small v_{SD})

$v_{OUT} > v_{IN}+|V_{tp}|$

$v_{OUT} = R_D k_p(V_{DD}-v_{IN}-|V_{tp}|)(V_{DD}-v_{OUT})$

$v_{OUT} = V_{DD}/(1+1/(R_D k_p(V_{DD}-v_{IN}-|V_{tp}|)))$

Saturation

$v_{OUT} < v_{IN}+|V_{tp}|$

$v_{OUT} = 0.5 R_D k_p((V_{DD}-|V_{tp}|)-v_{IN})^2$

$v_{OUT} = 0.5 R_D k_p(v_{IN}-(V_{DD}-|V_{tp}|))^2$

Cutoff

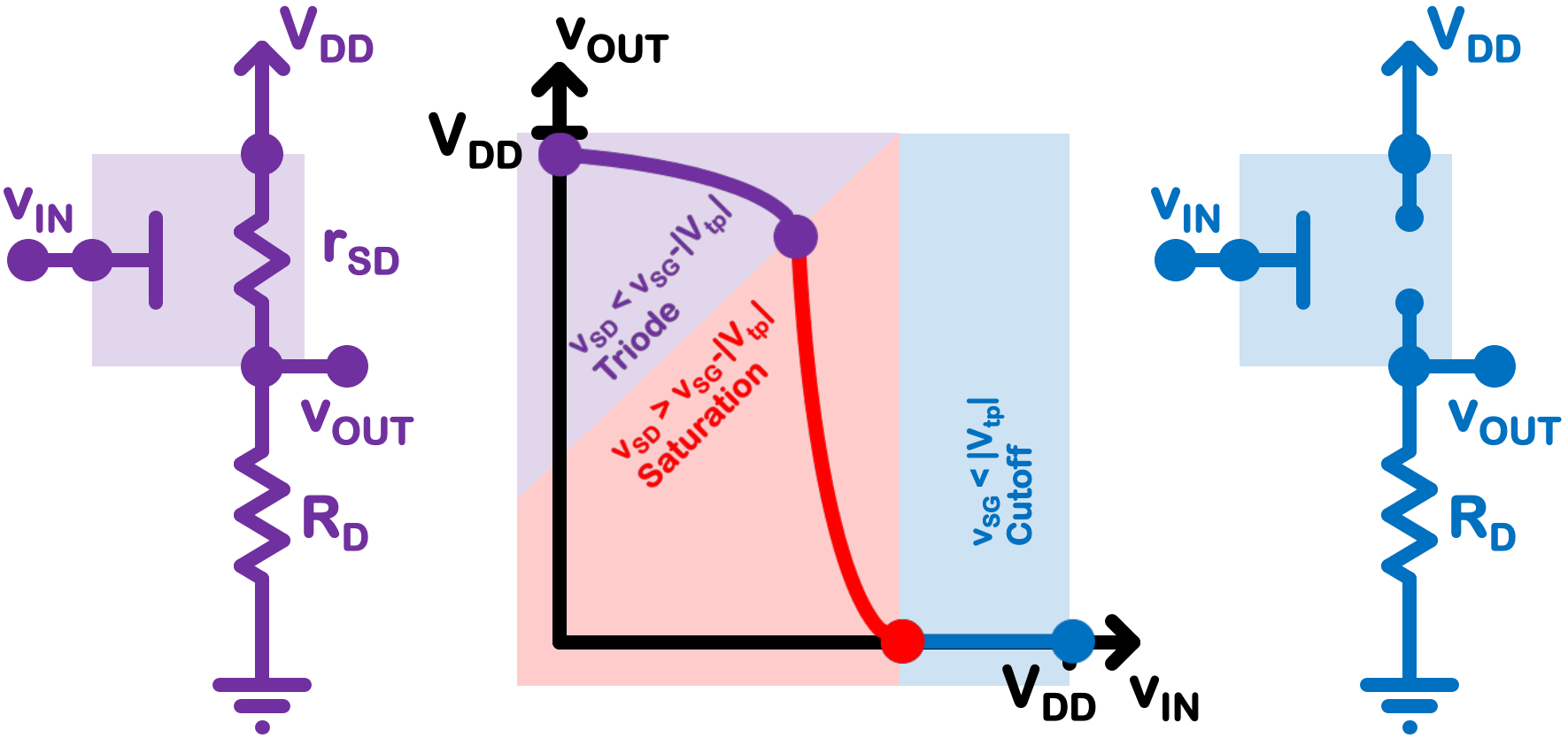
$v_{IN} > V_{DD}-|V_{tp}|$

$v_{OUT} = 0$

PMOS Inverter (models)

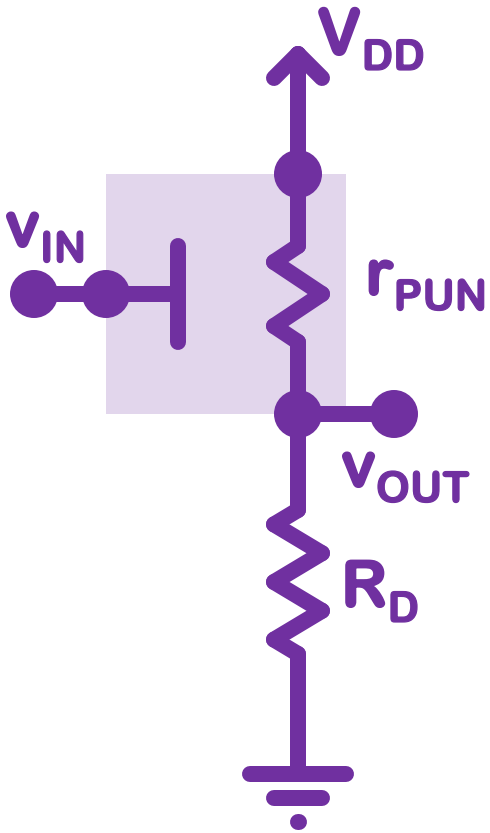
At $v_{IN}=0$

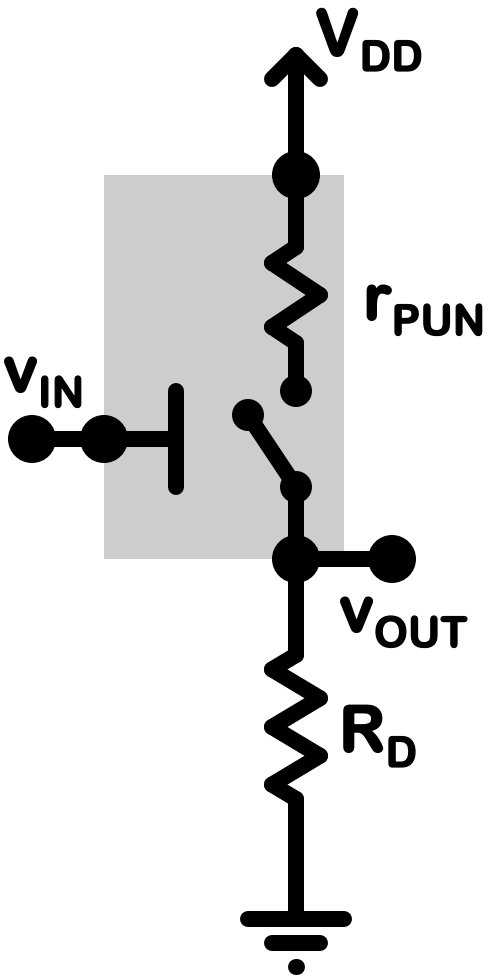
$r_{SD} = 1/(k_p(V_{DD}-|V_{tp}|))$



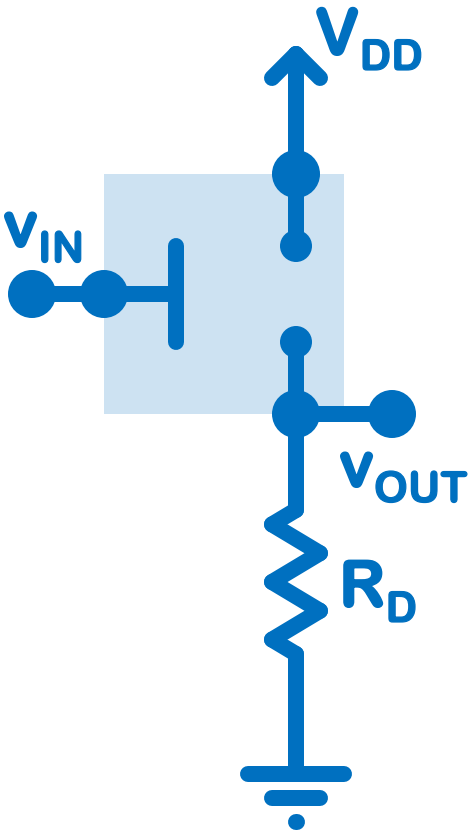
Basic Inverter
PMOS Inspired

v_{IN} is LOW,
Switch is CLOSED,
Conducting,
v_{OUT} is HIGH.





v_{IN} is HIGH,
Switch is OPEN.
Not Conducting,
v_{OUT} is LOW.

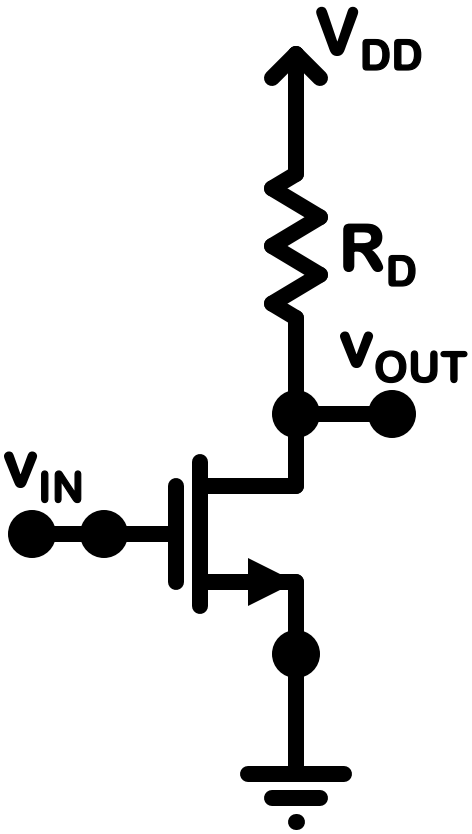


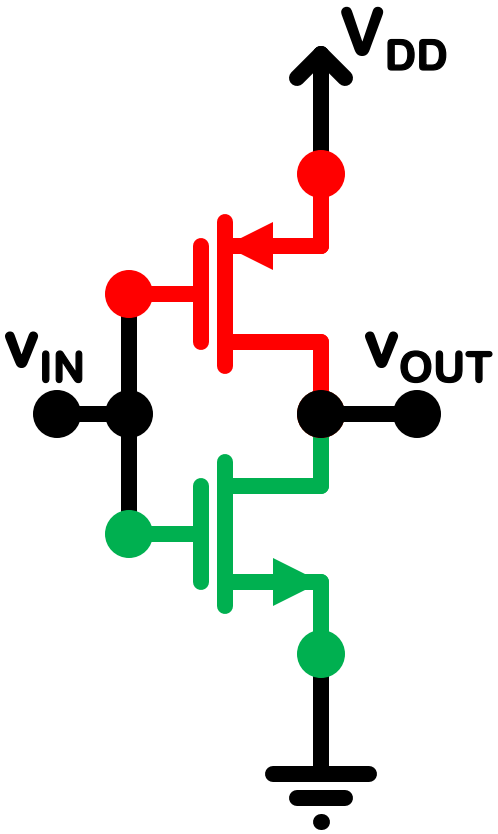
$r_{PUN} = r_{SD} = 1/(k_p(v_{DD}-|V_{tp}|))$

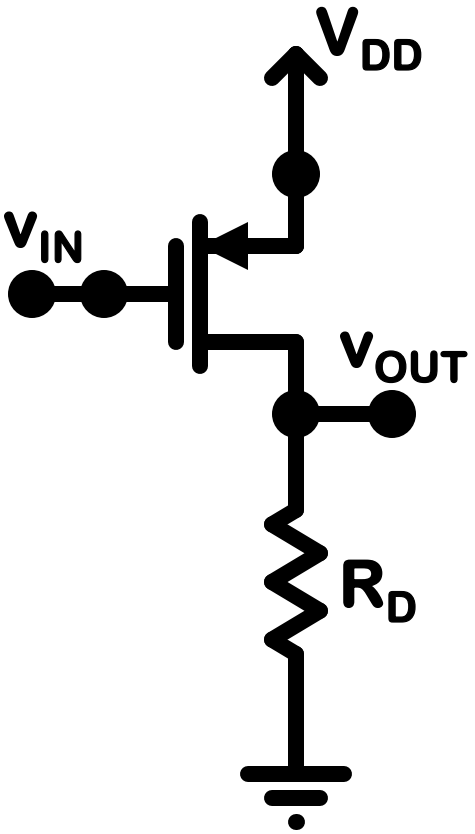
$P_D=V_{DD}^2/(R_D+r_{PUN})$

$P_D=0$

CMOS Inverter

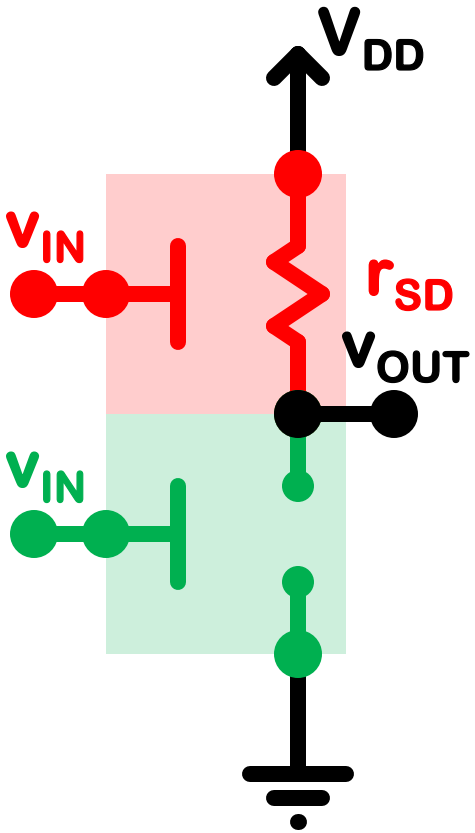


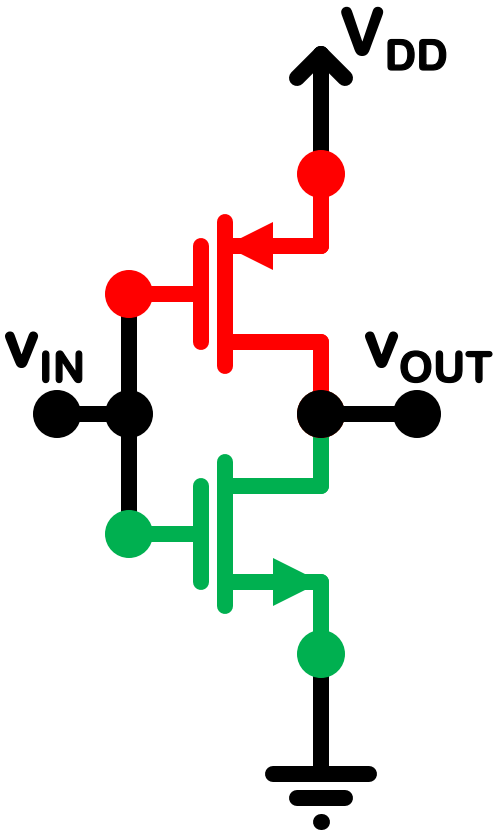


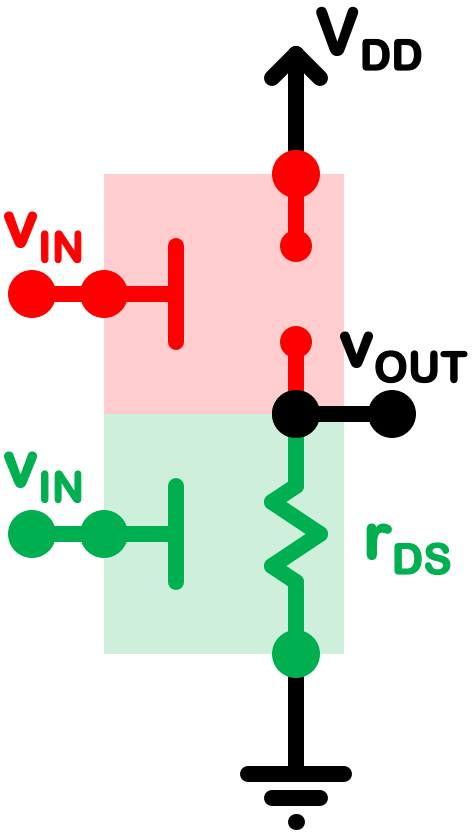


CMOS Inverter (models)

At $v_{IN}=0$
$r_{SD} = 1/(k_p(v_{DD}-|V_{tp}|))$



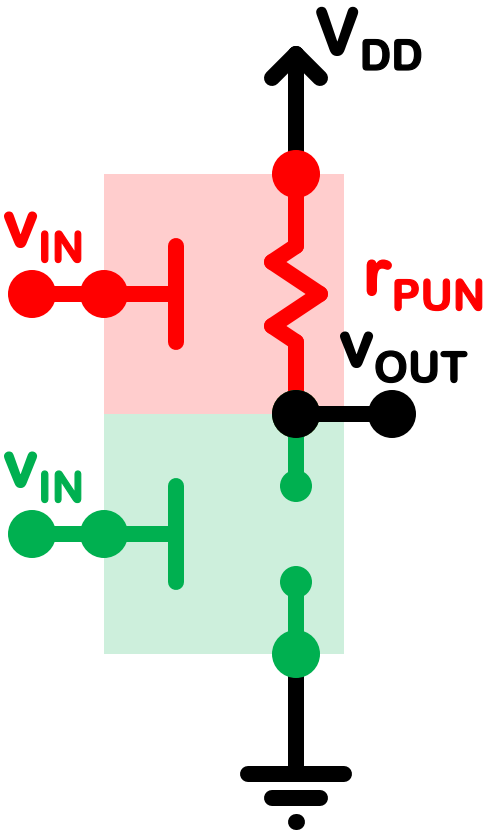




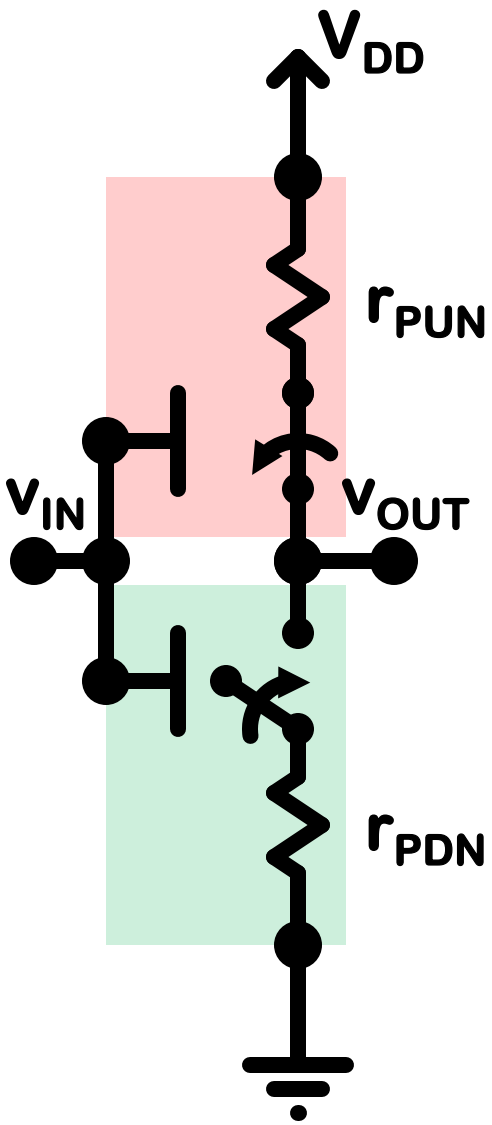
At $v_{IN}=V_{DD}$
$r_{DS} = 1/(k_n(v_{DD}-V_{tn}))$

Basic Inverter
CMOS Inspired

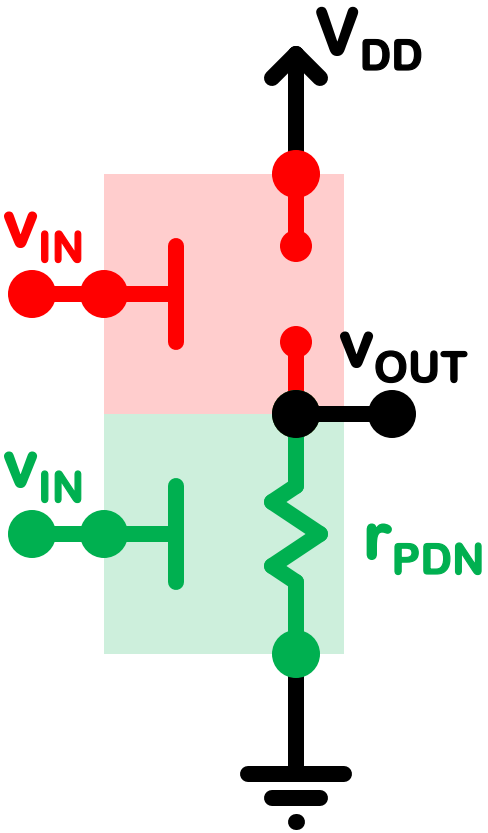
v_{IN} is LOW,
PMOS is conducting,
v_{OUT} is HIGH.



P_D=0



v_{IN} is HIGH,
NMOS is conducting,
v_{OUT} is LOW.



P_D=0