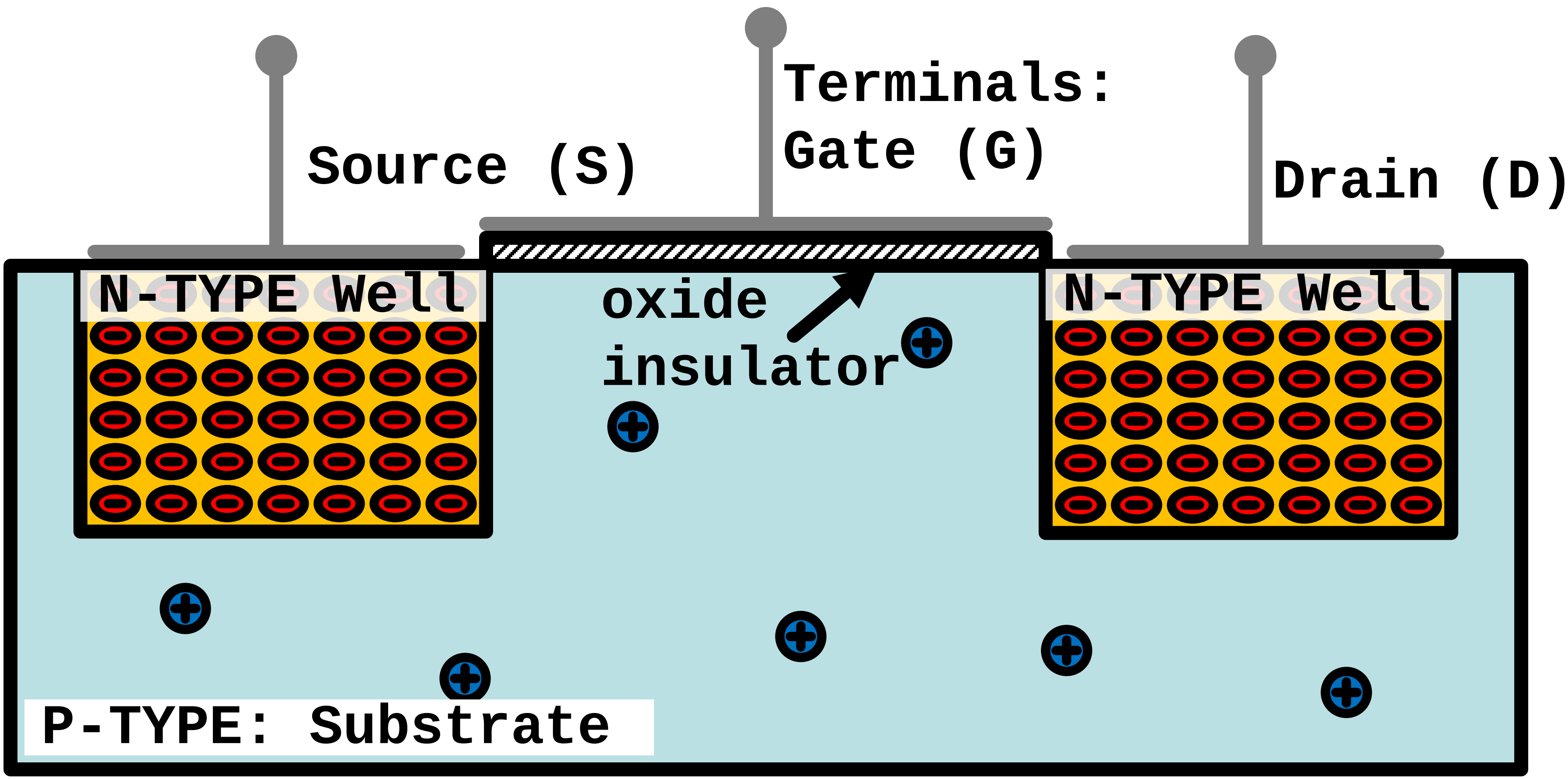
MOSFET - Structure

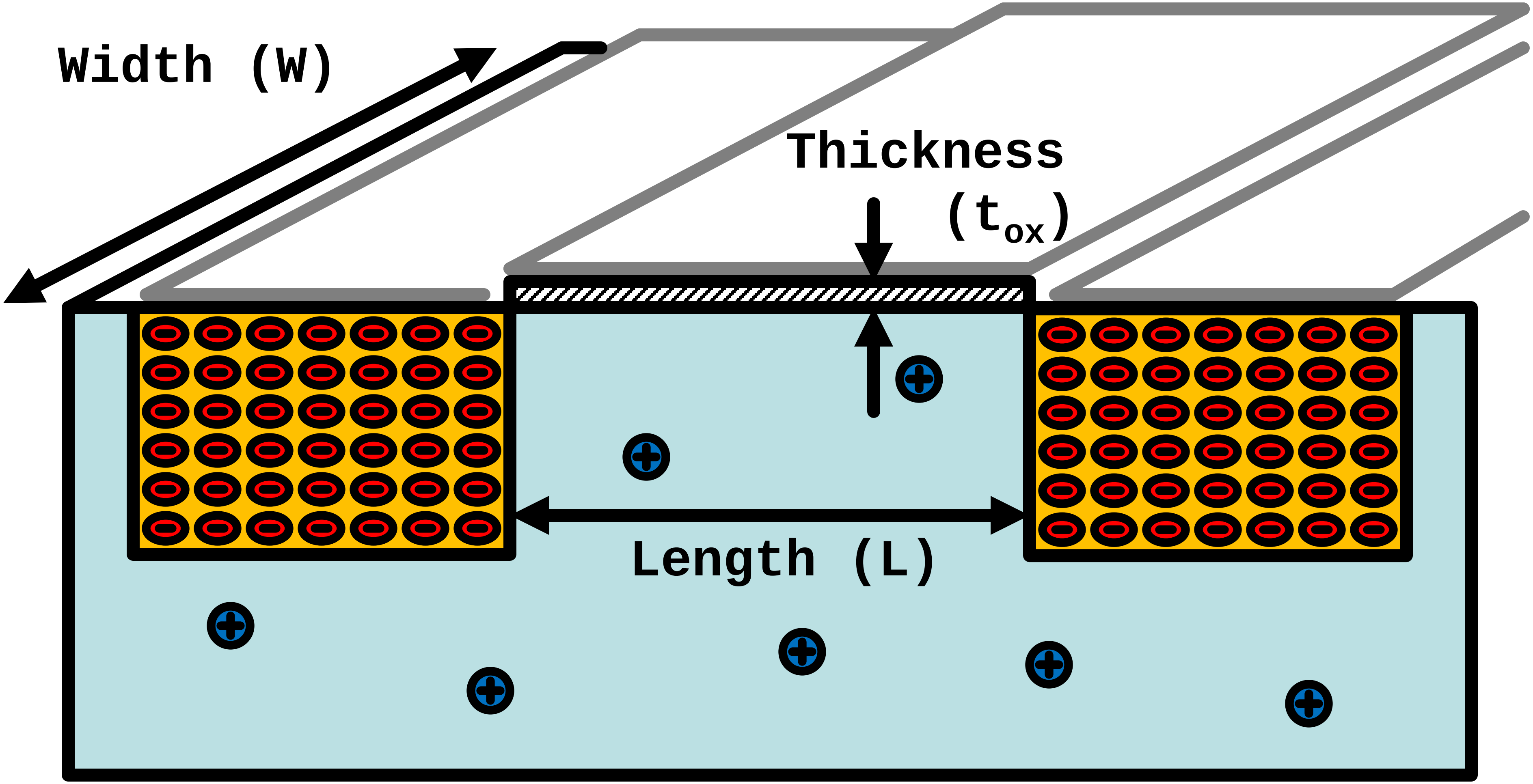
Properties

Oxide Insulator: $\varepsilon_{ox}=$

N-Type: $\mu_n=$

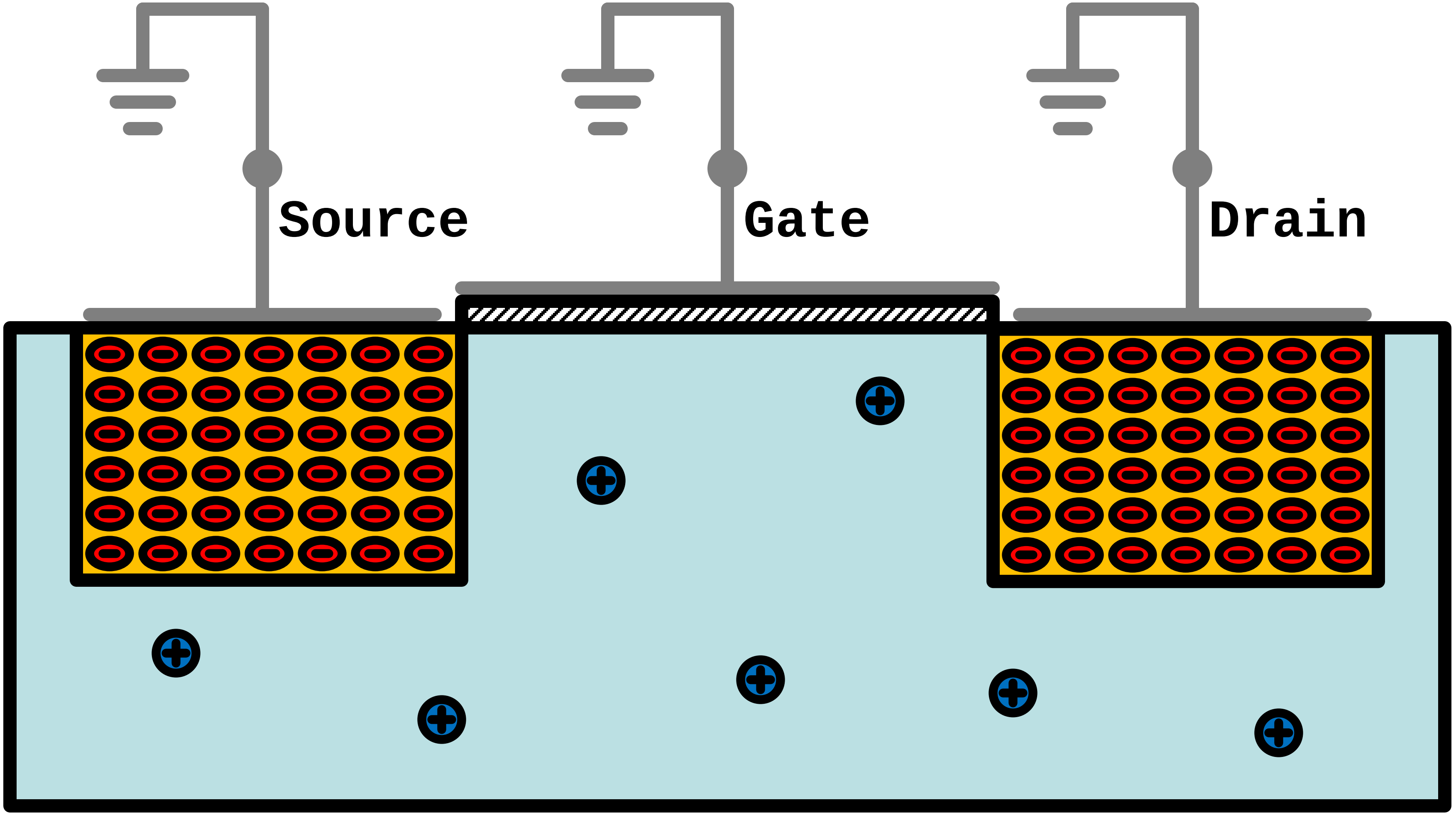


MOSFET - Dimensions

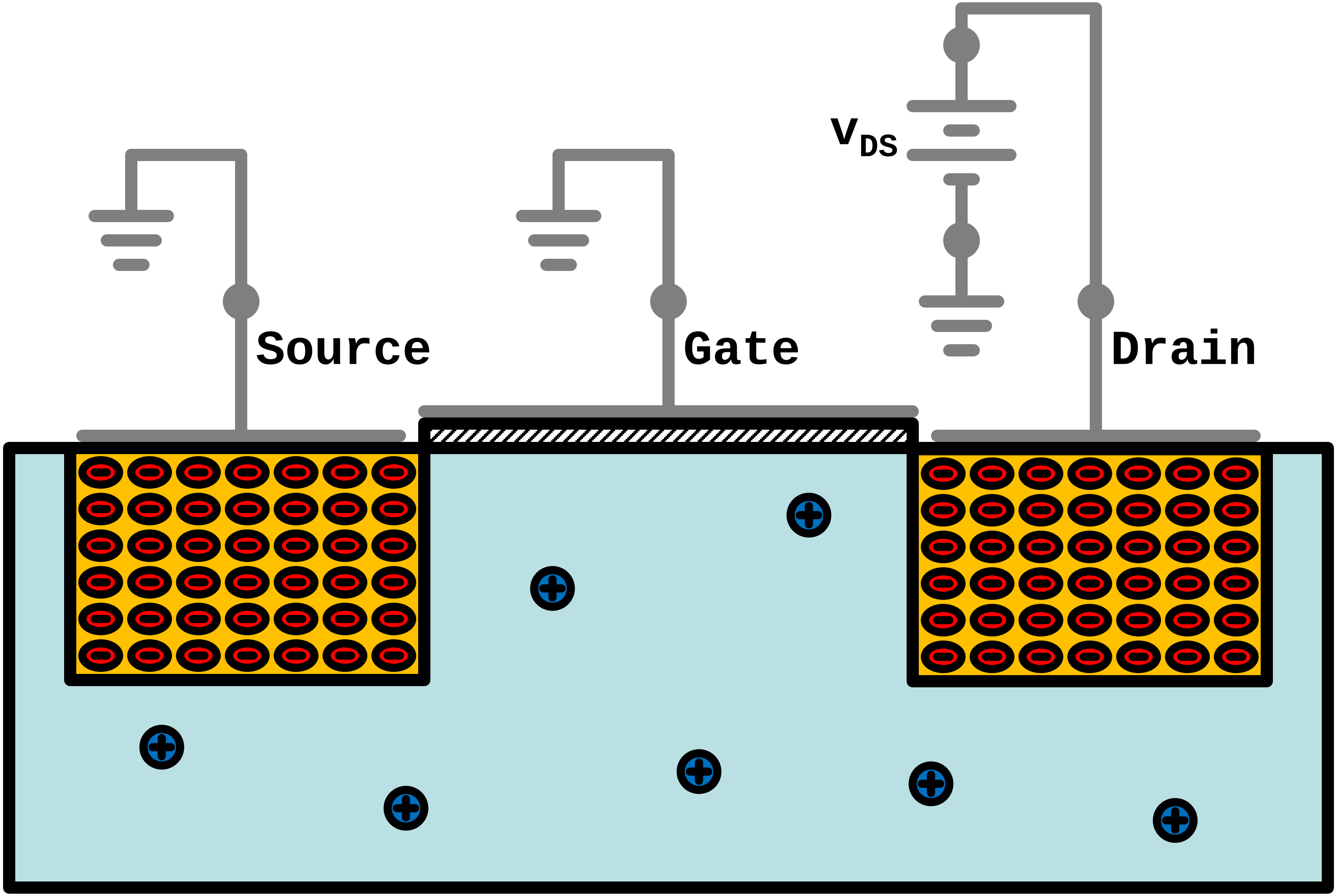


MOSFET – Operation and Modes

No current flows into the gate.
Try to make current flow into the drain.

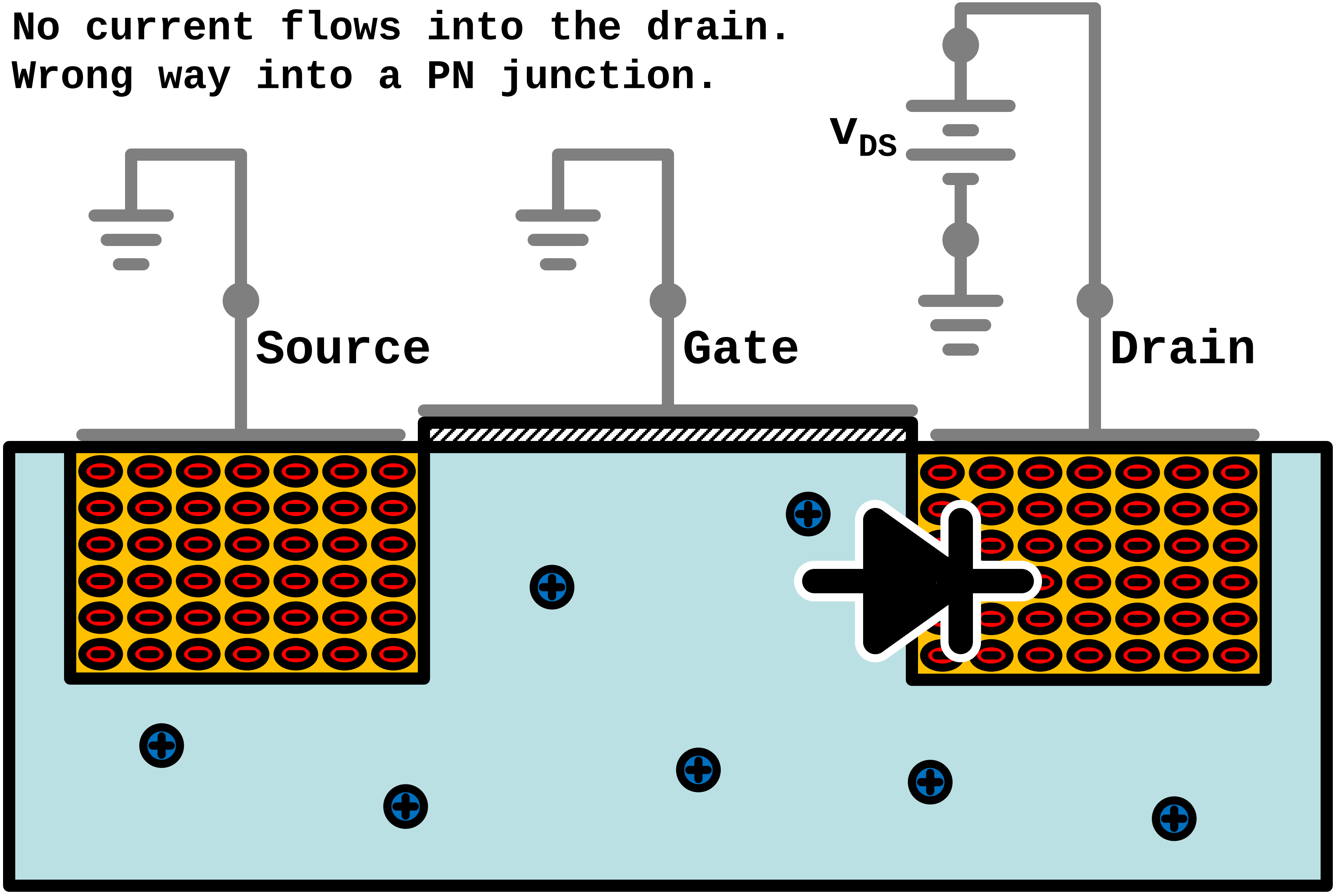


MOSFET – Operation and Modes



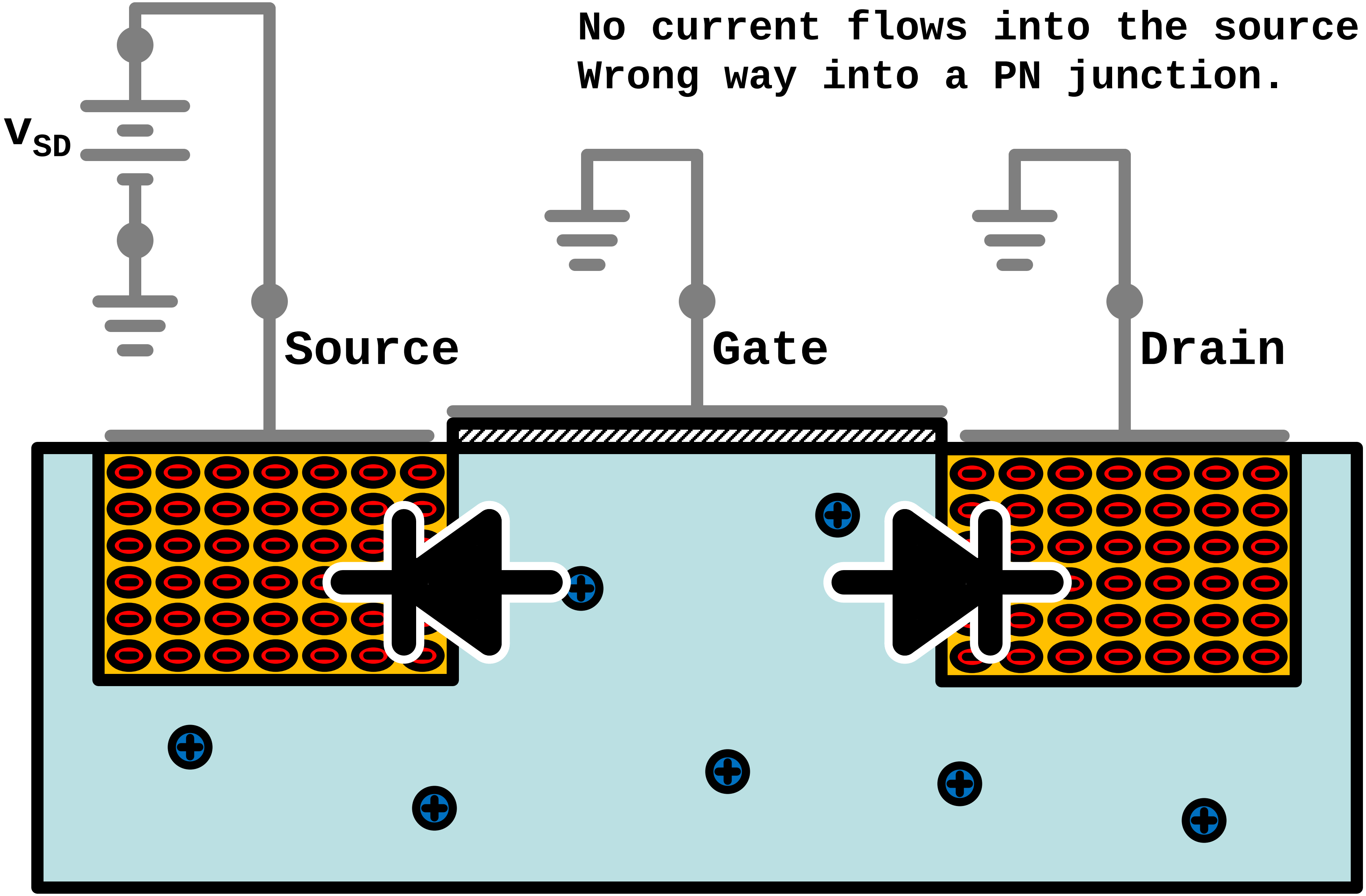
MOSFET – Operation and Modes

No current flows into the drain.
Wrong way into a PN junction.



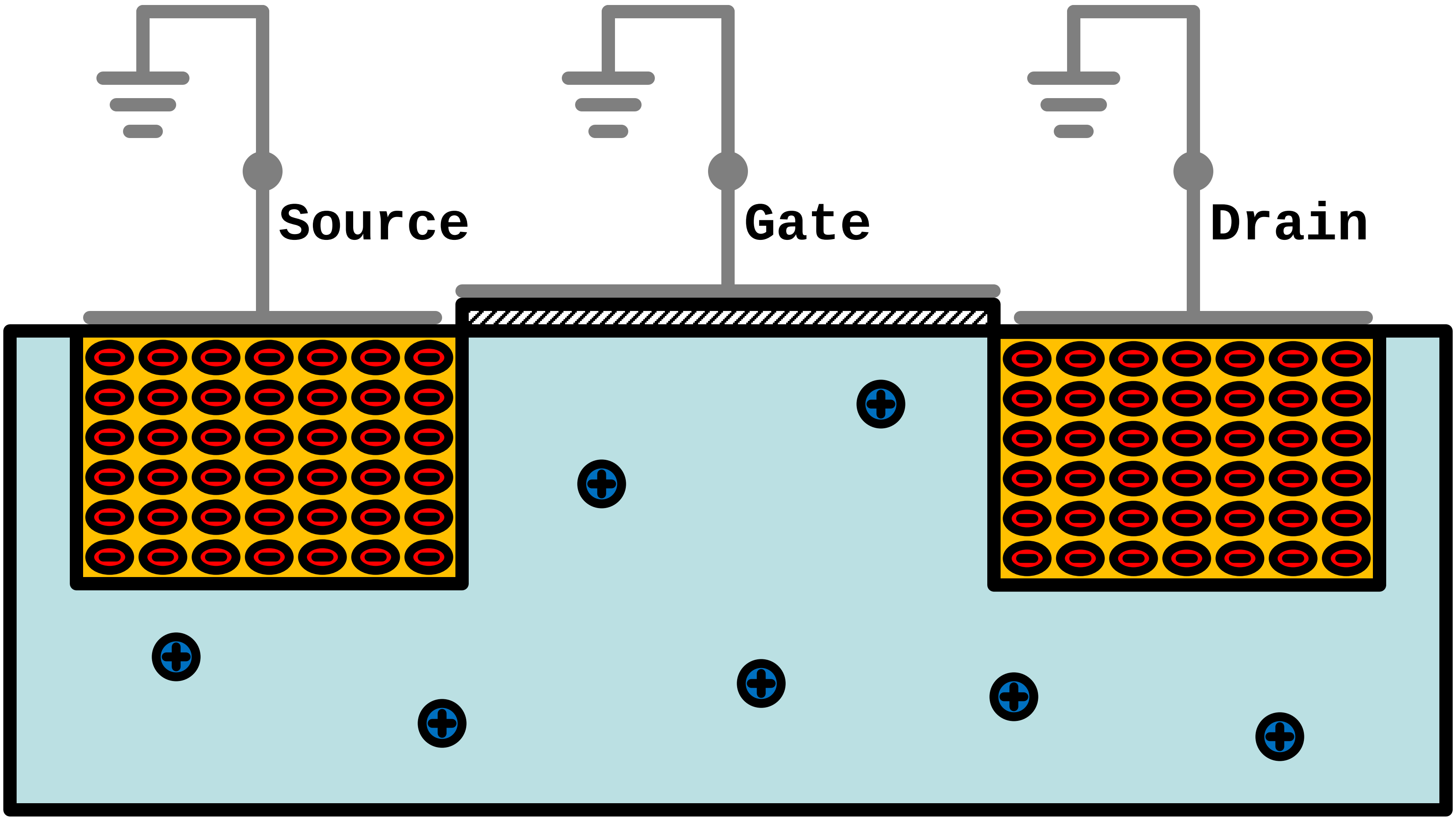
MOSFET – Operation and Modes

No current flows into the source.
Wrong way into a PN junction.

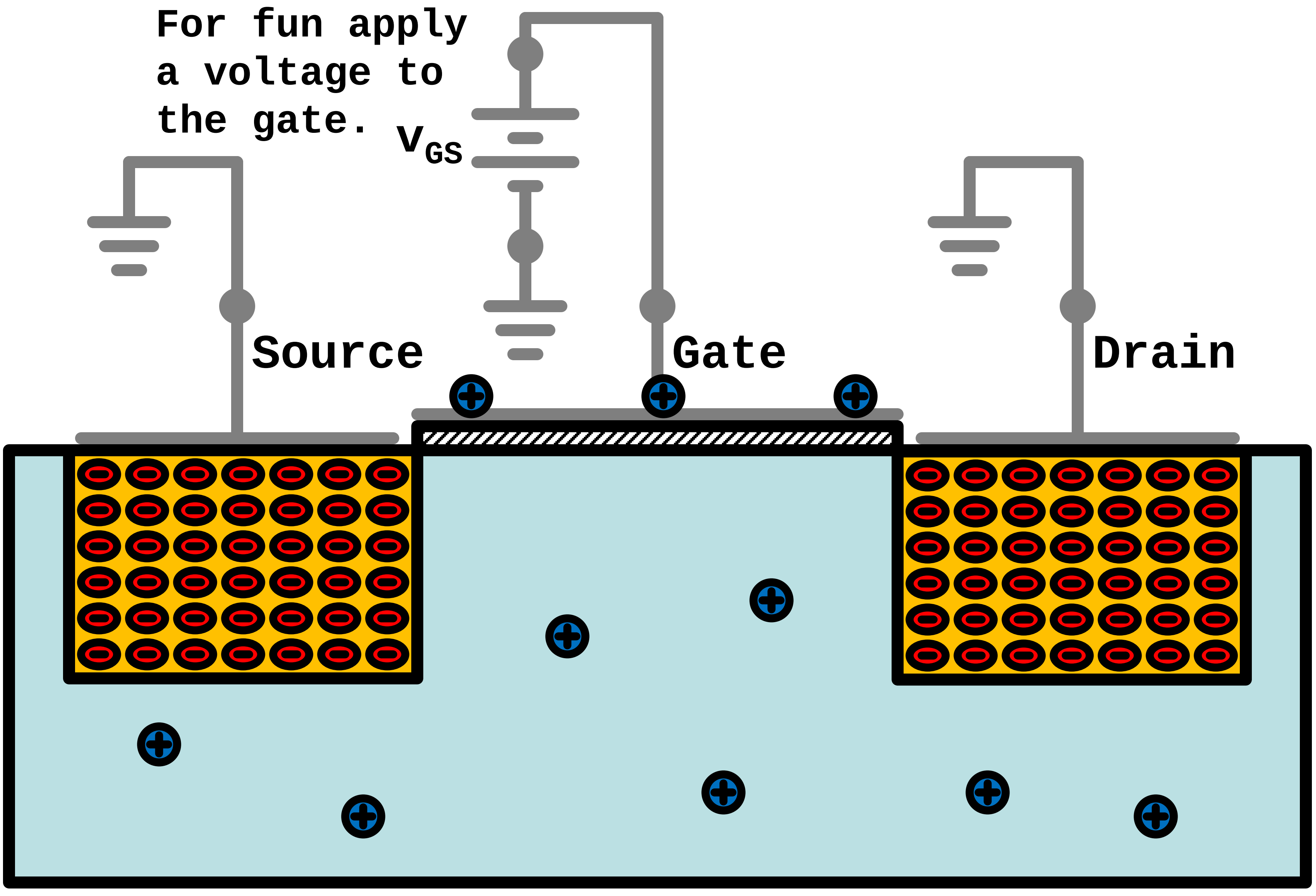


MOSFET – Operation and Modes

For fun apply a voltage to the gate.

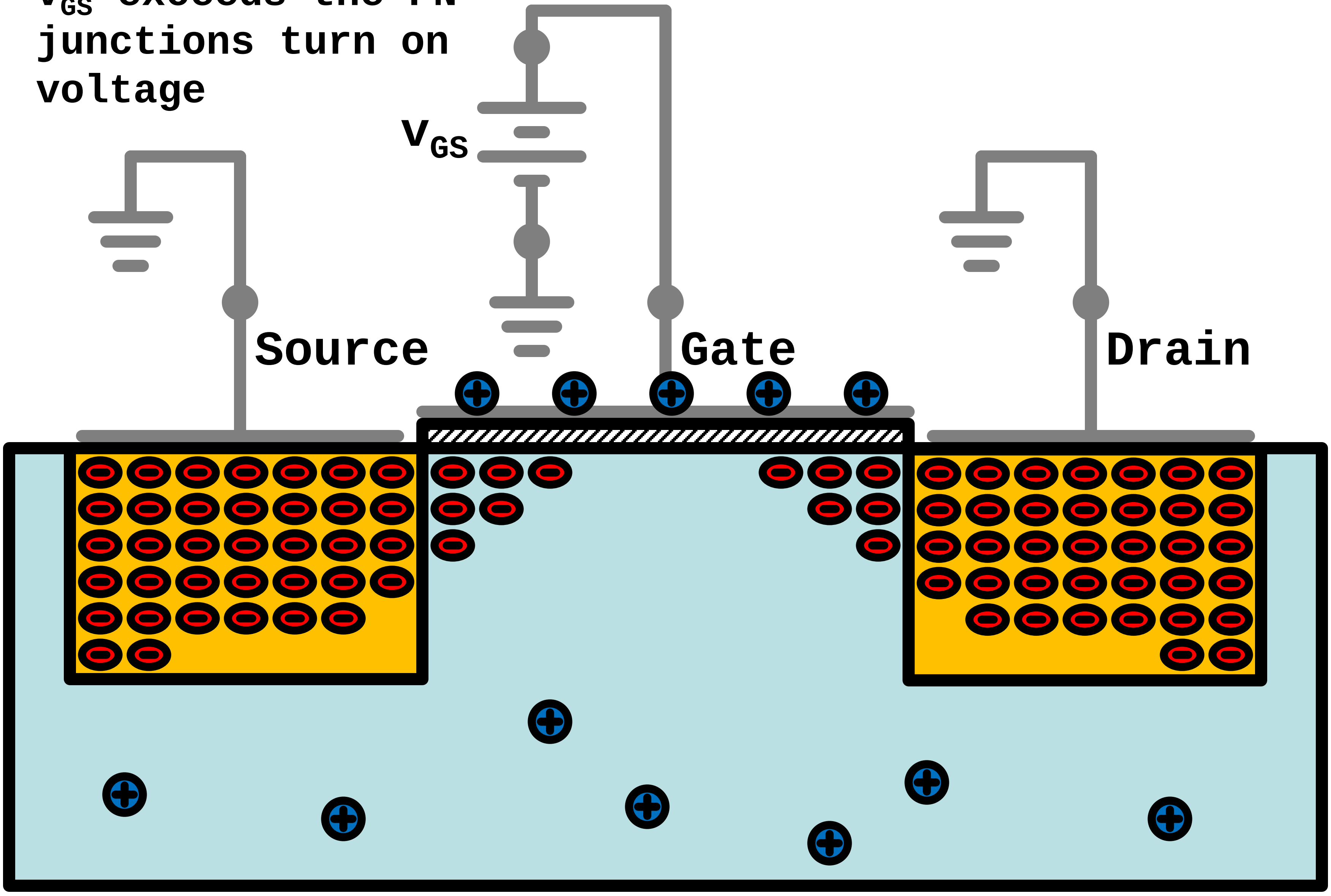


MOSFET – Operation and Modes



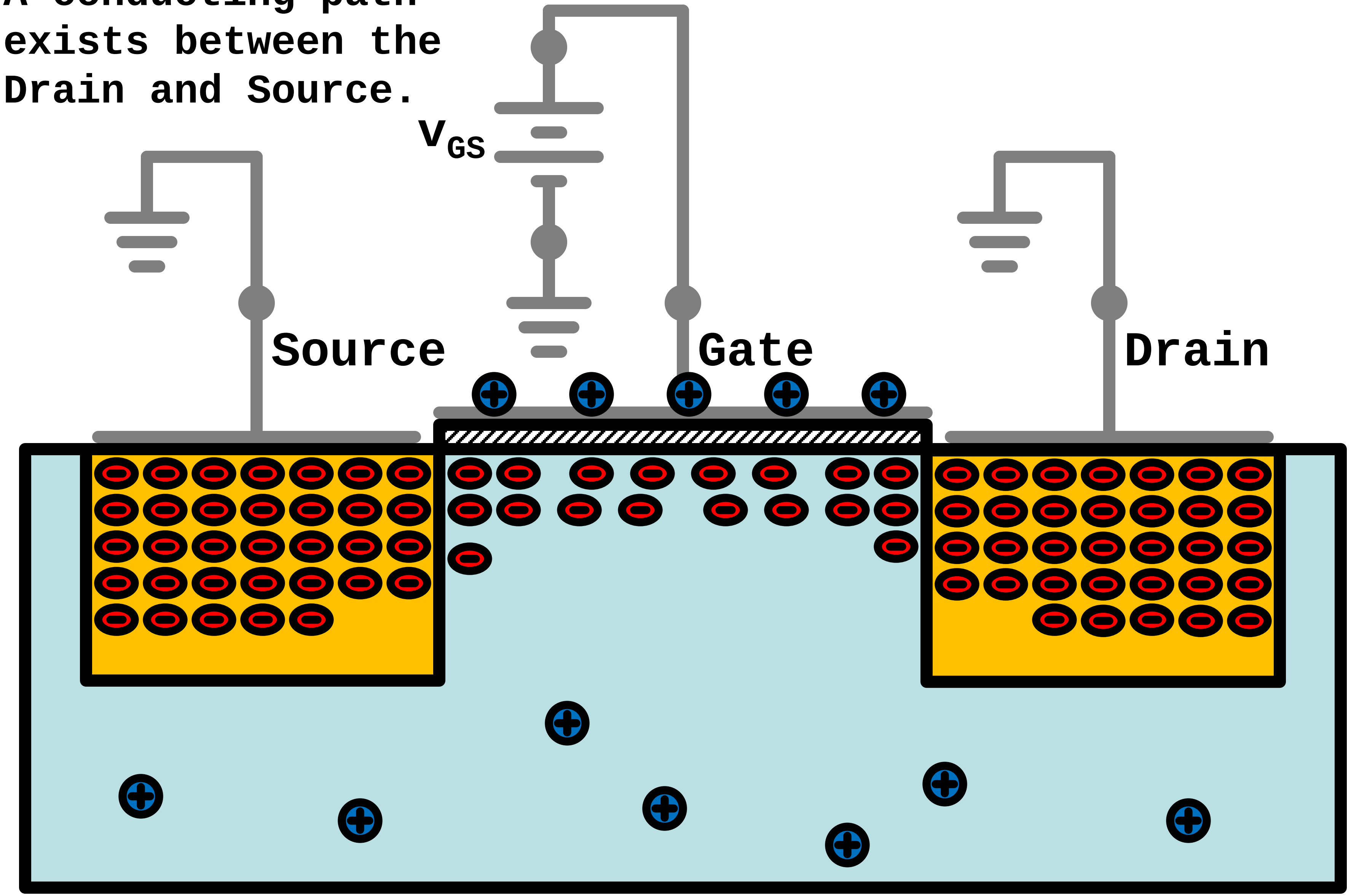
MOSFET – Operation and Modes

V_{GS} exceeds the PN junctions turn on voltage



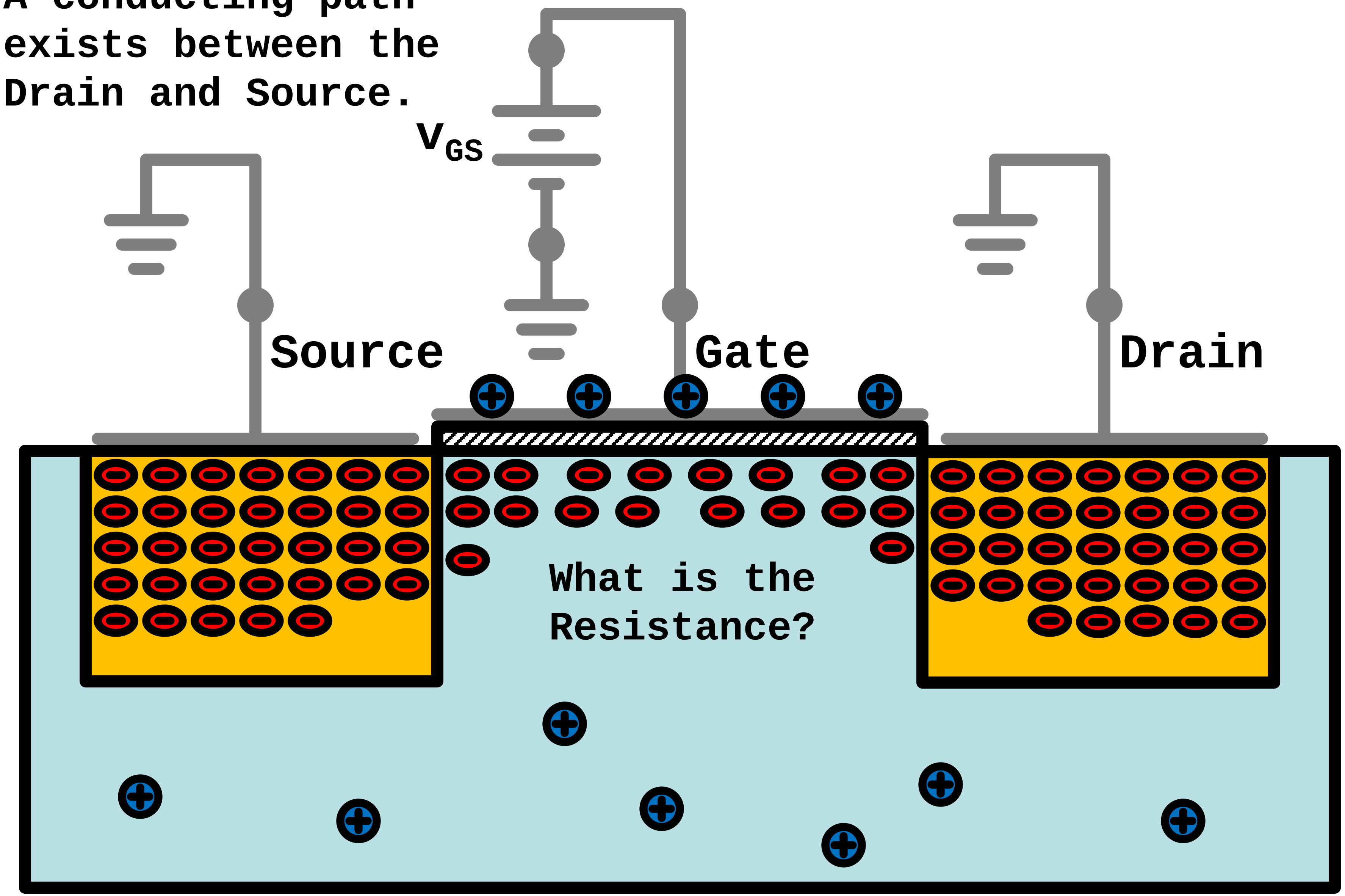
MOSFET – Operation and Modes

A conducting path exists between the Drain and Source.



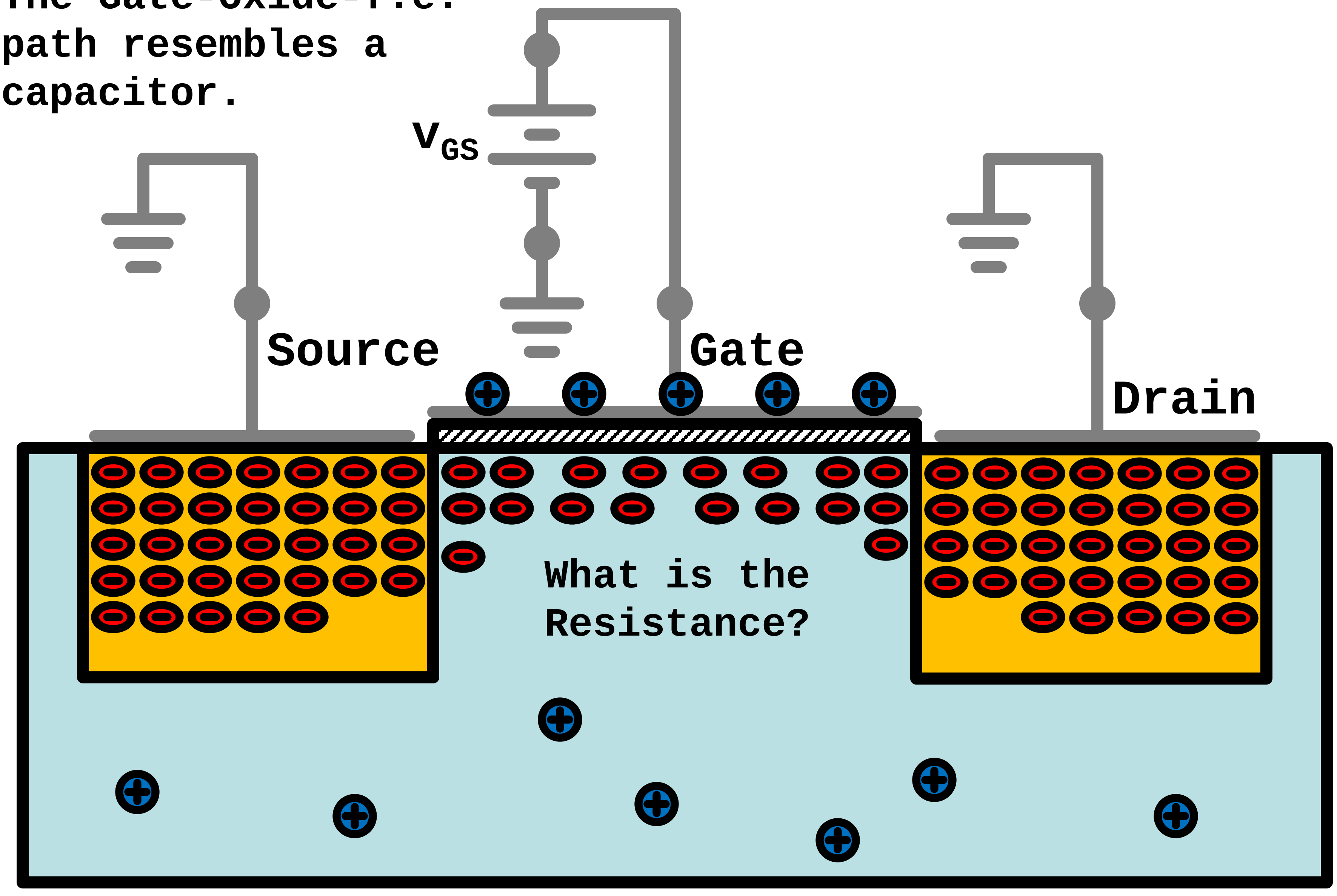
MOSFET – Operation and Modes

A conducting path exists between the Drain and Source.



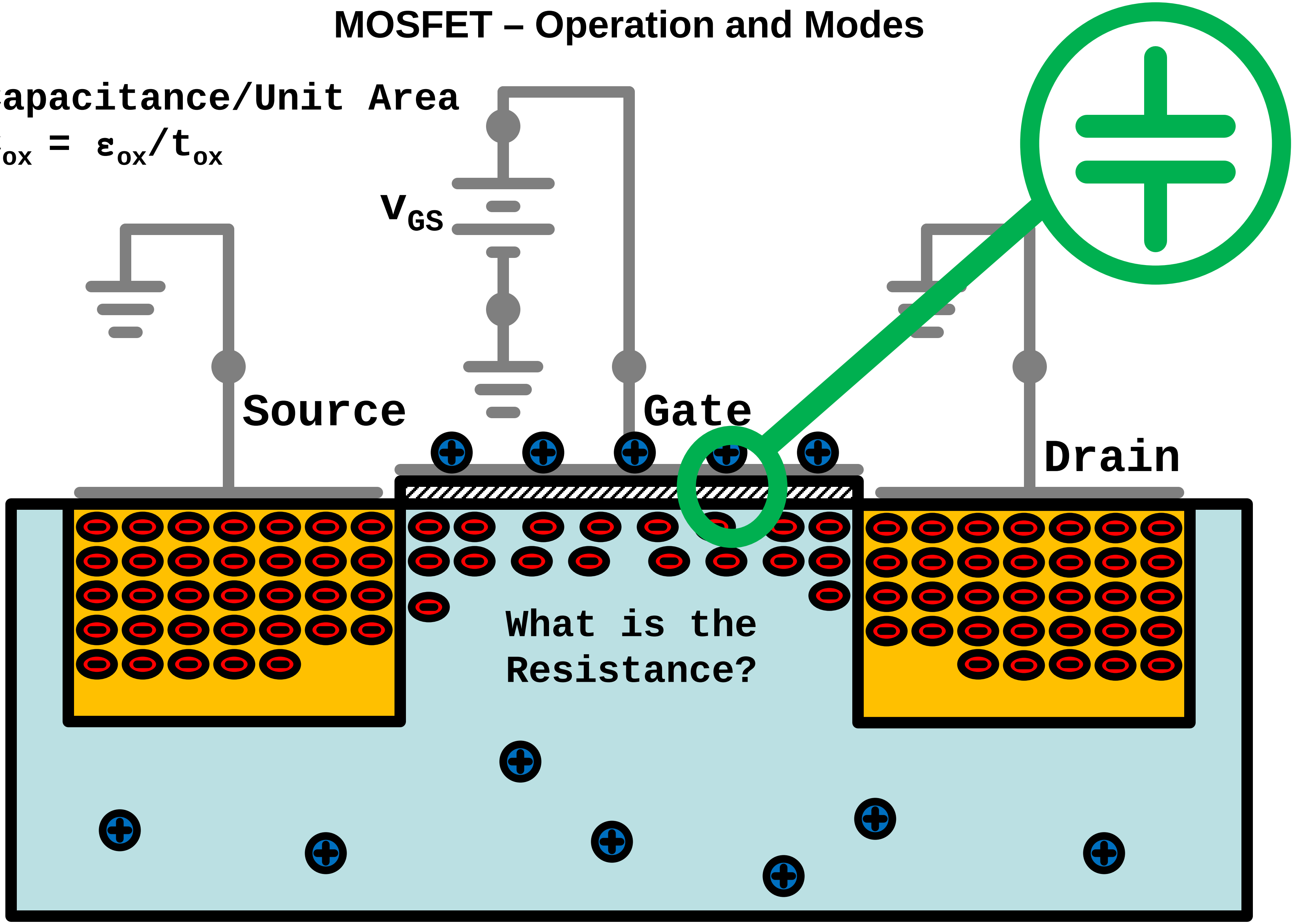
MOSFET – Operation and Modes

The Gate-Oxide-f.e. path resembles a capacitor.



MOSFET – Operation and Modes

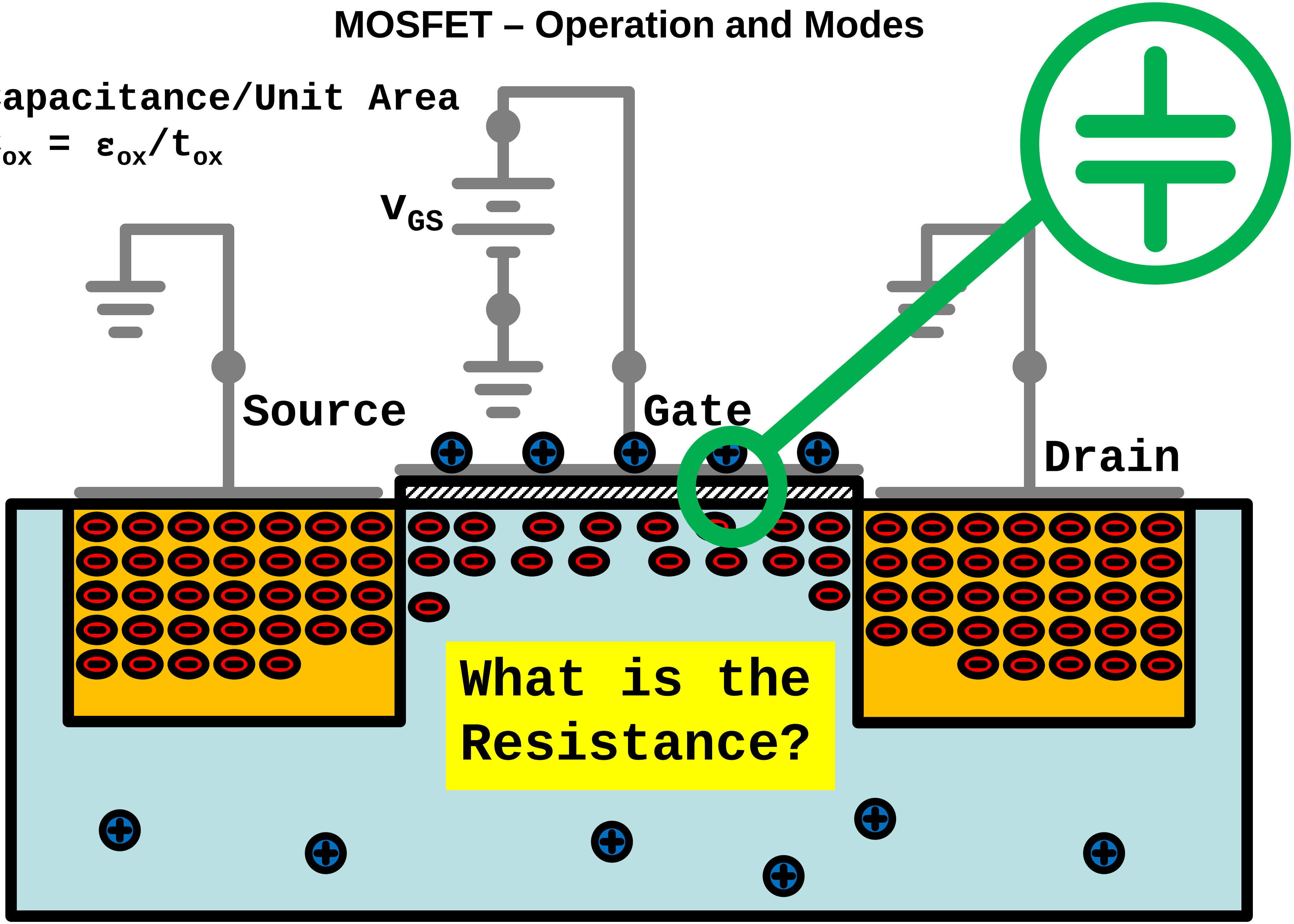
Capacitance/Unit Area
$C_{ox} = \varepsilon_{ox}/t_{ox}$



MOSFET – Operation and Modes

Capacitance/Unit Area

$C_{ox} = \varepsilon_{ox}/t_{ox}$



Resistance Calculation

v_{GS} exceeds the PN junctions turn on voltage, V_t.

Resistance of uniform charge distribution:

R = Length/((mobility)·(charge per unit length))

Capacitance/Unit Area: $C_{ox} = \varepsilon_{ox}/t_{ox}$

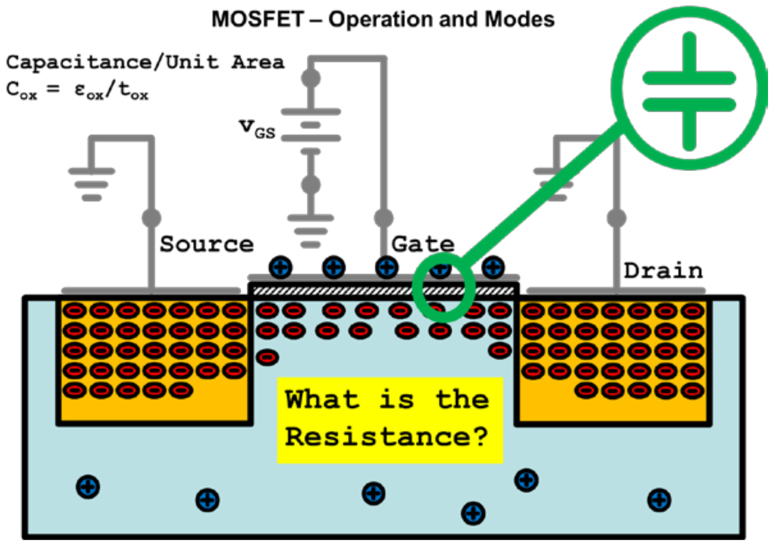
Area = W·L (from MOSFET Dimensions Slide)

Total Capacitance: $C = C_{ox} \cdot Area = (C_{ox} \cdot W \cdot L)$

Total Charge ($Q=C \cdot V$): $Q = (C_{ox} \cdot W \cdot L) \cdot (v_{GS}-V_t)$

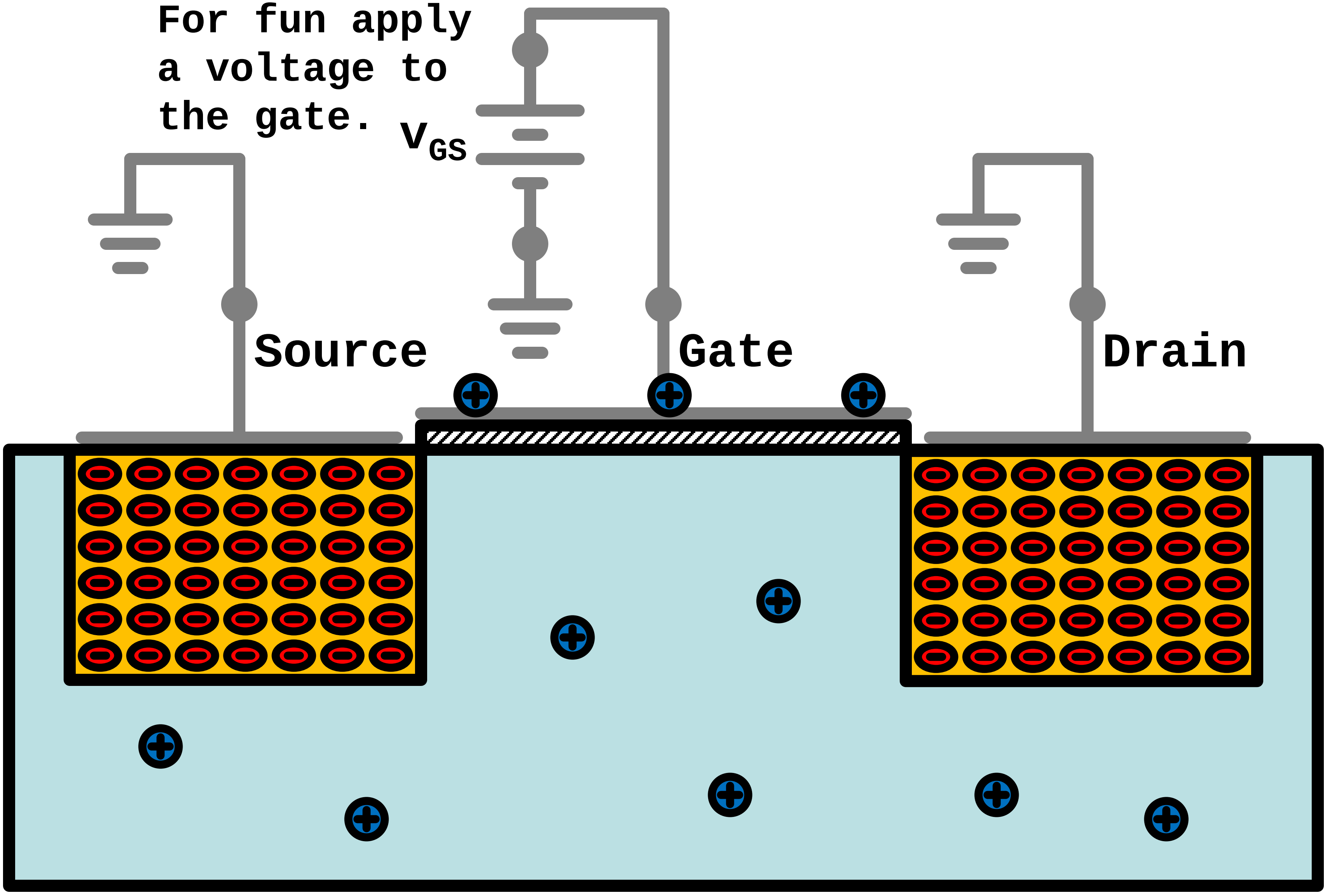
charge per unit length = $Q/L = (C_{ox} \cdot W) \cdot (v_{GS}-V_t)$

$$R = L/(\mu_n \cdot C_{ox} \cdot W \cdot (v_{GS}-V_t))$$



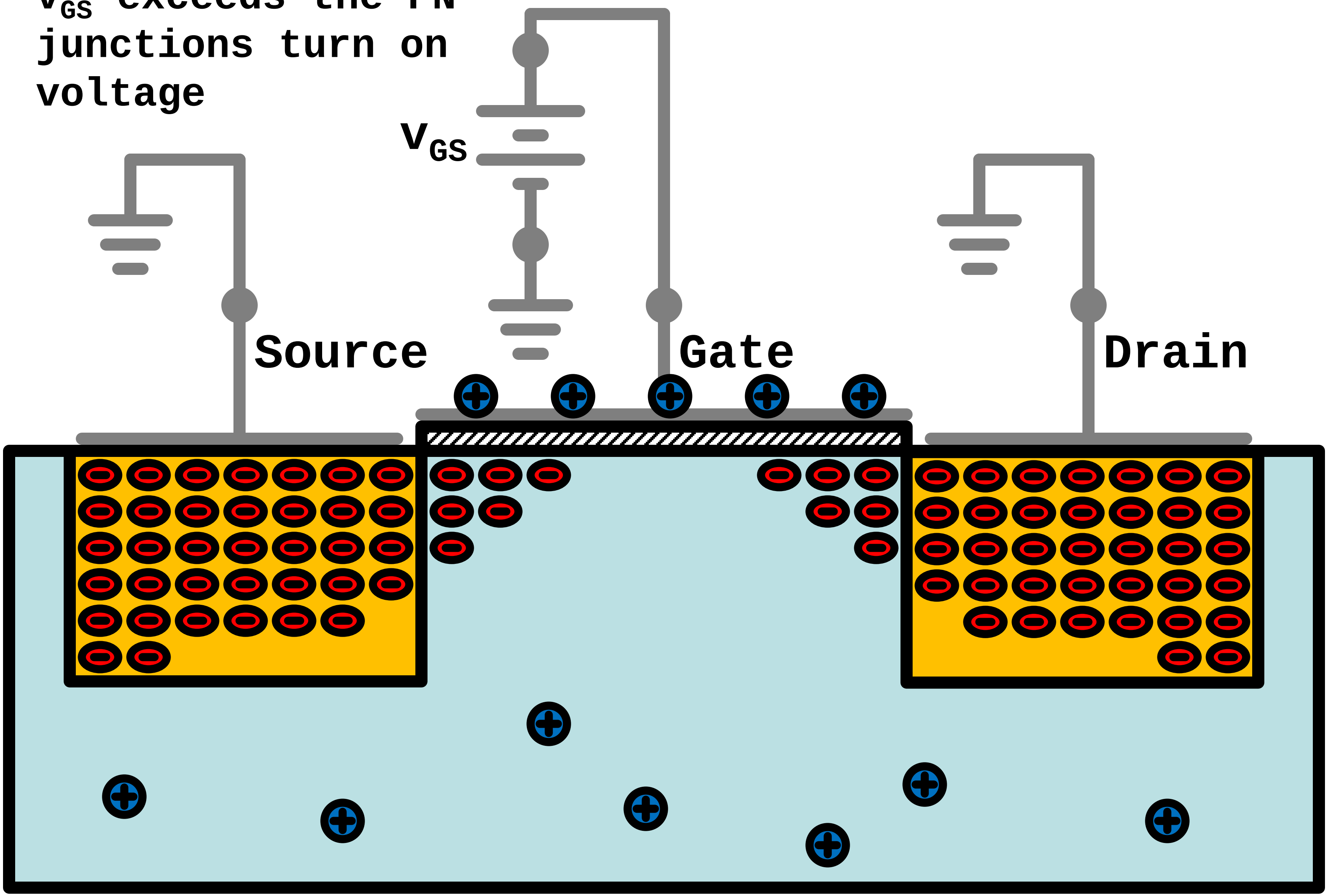
MOSFET – Review channel shape

For fun apply a voltage to the gate.



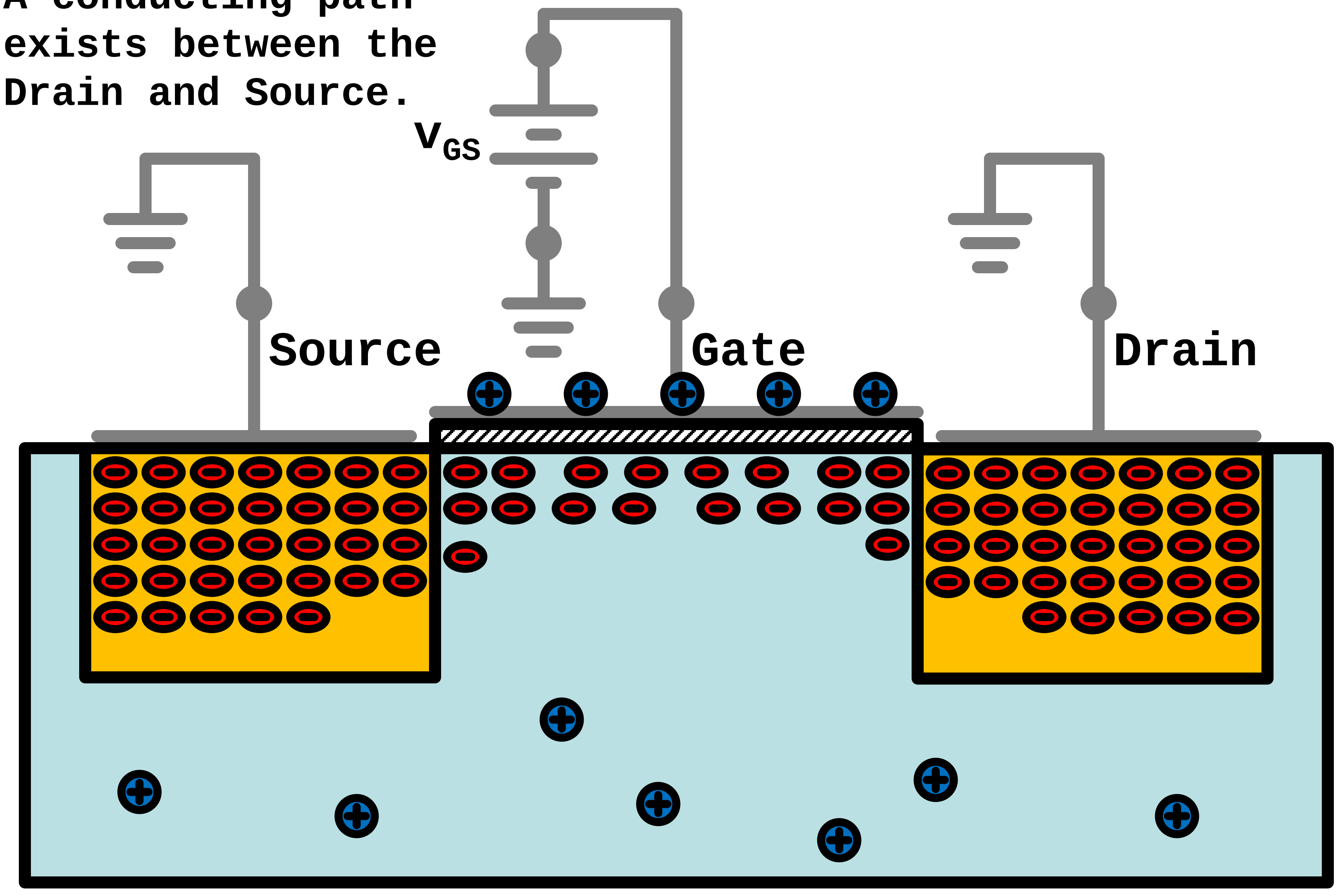
MOSFET – Operation and Modes

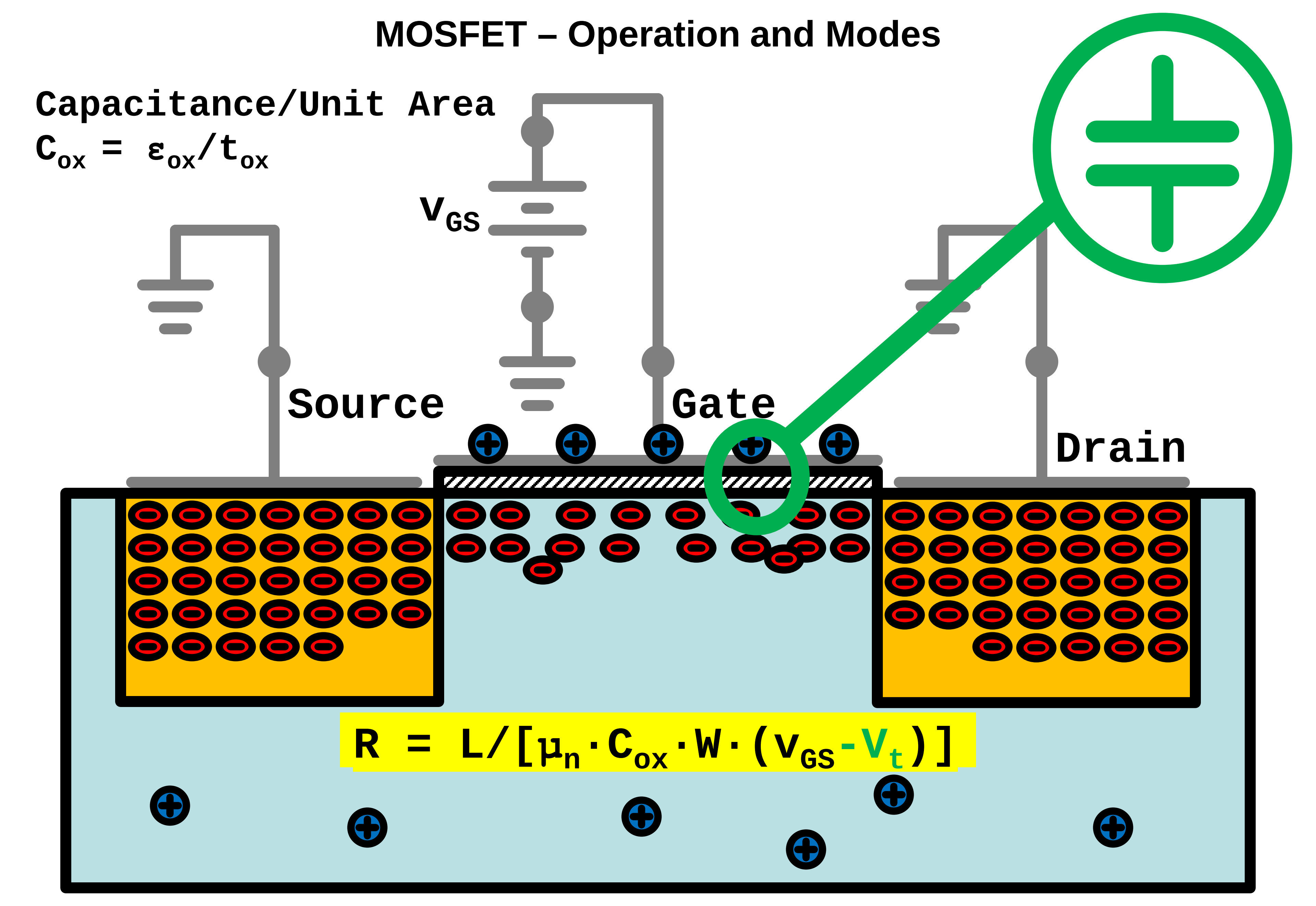
V_{GS} exceeds the PN junctions turn on voltage



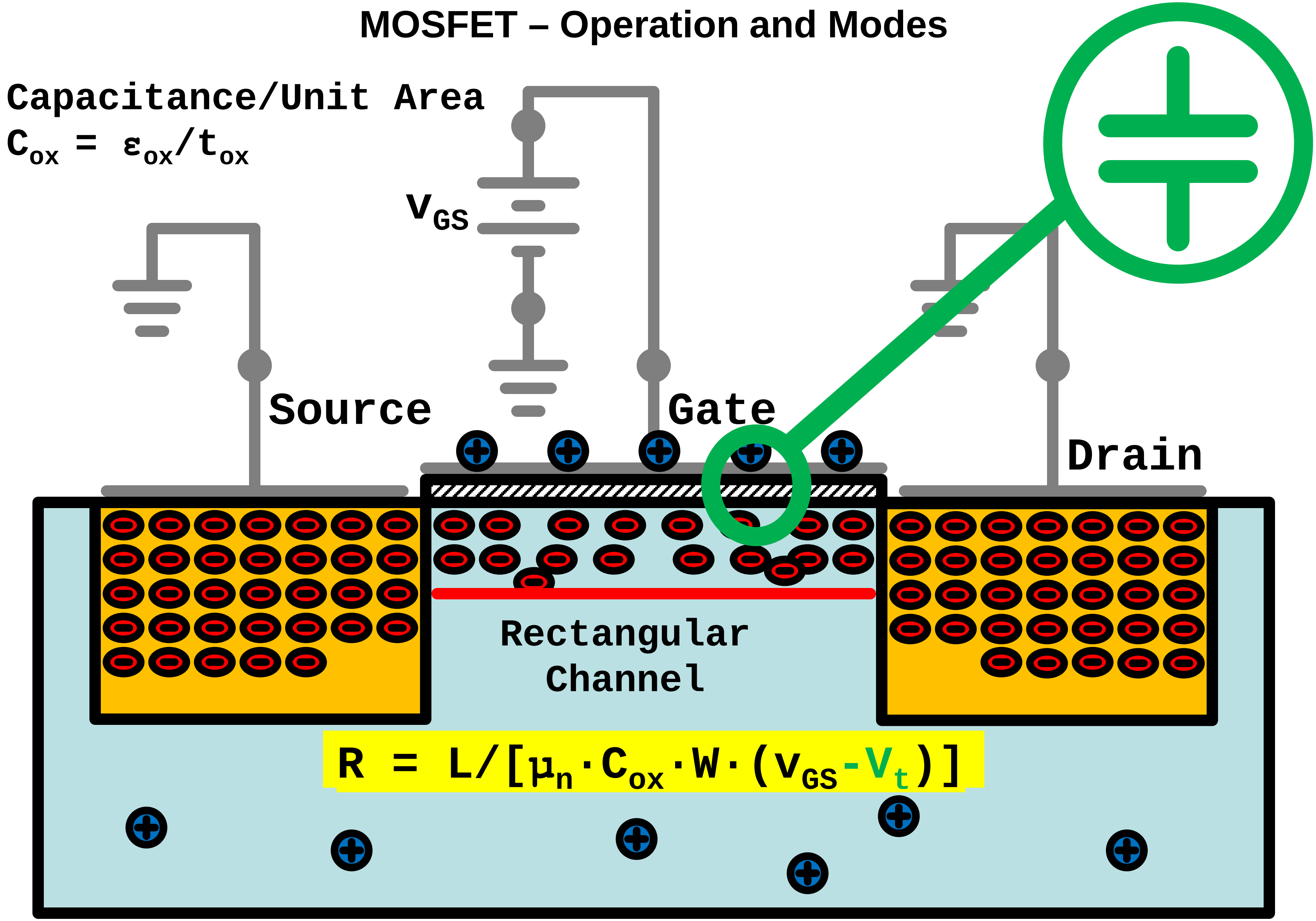
MOSFET – Operation and Modes

A conducting path exists between the Drain and Source.

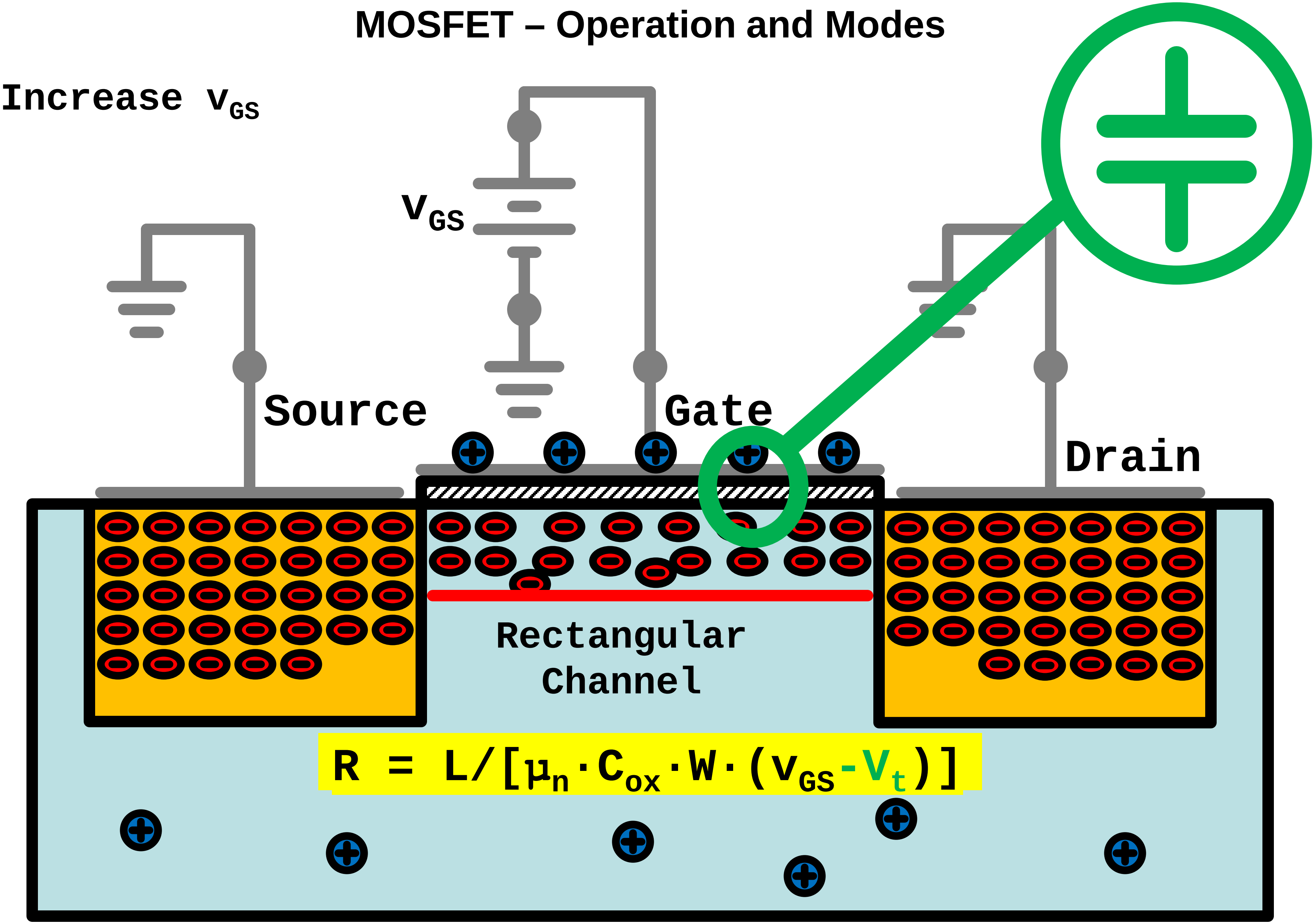



MOSFET – Operation and Modes
Capacitance/Unit Area
$C_{ox} = \varepsilon_{ox}/t_{ox}$
v_{GS}
Source
Gate
Drain
$R = L/[\mu_n \cdot C_{ox} \cdot W \cdot (v_{GS} - V_t)]$

MOSFET – Operation and Modes

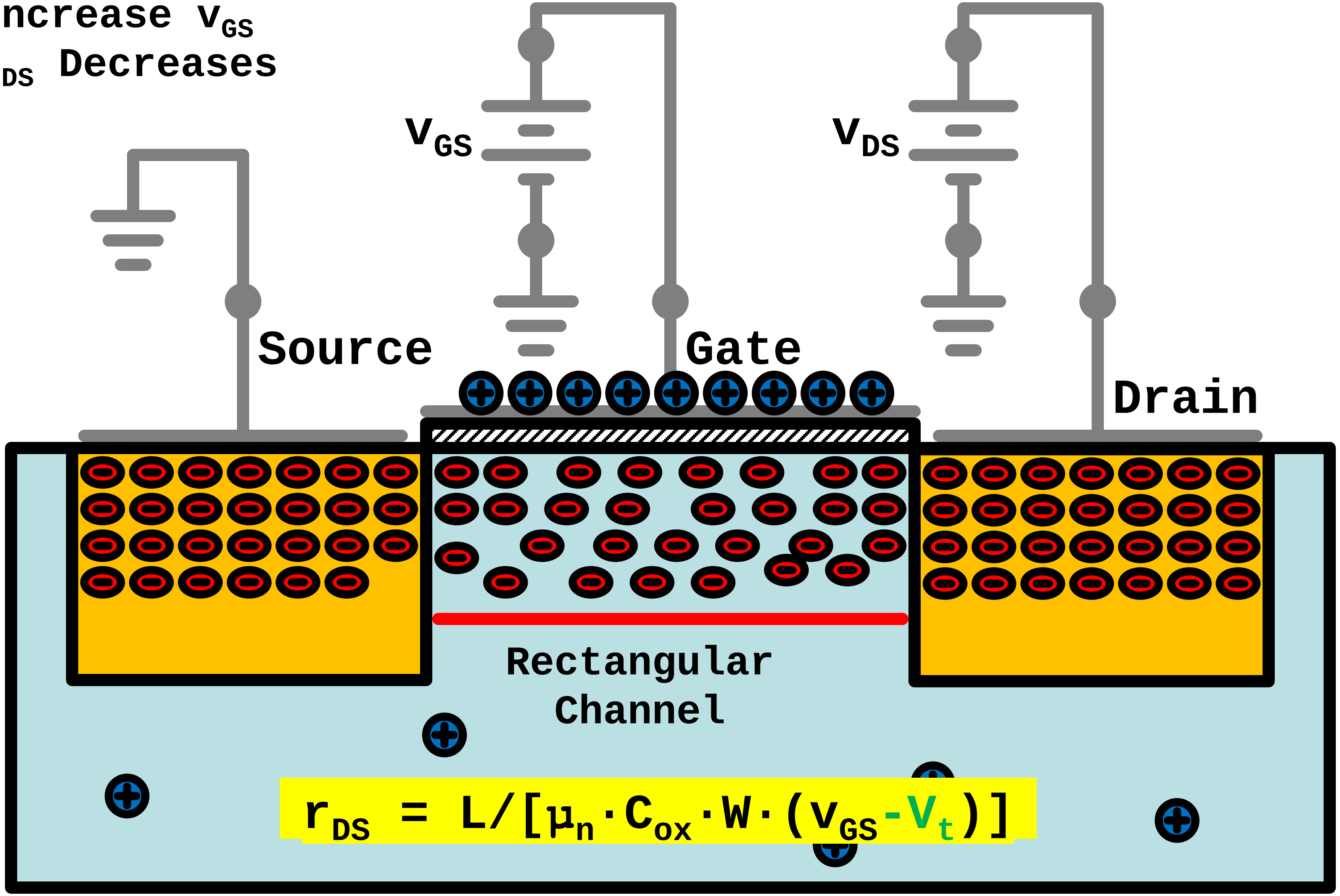


MOSFET – Operation and Modes



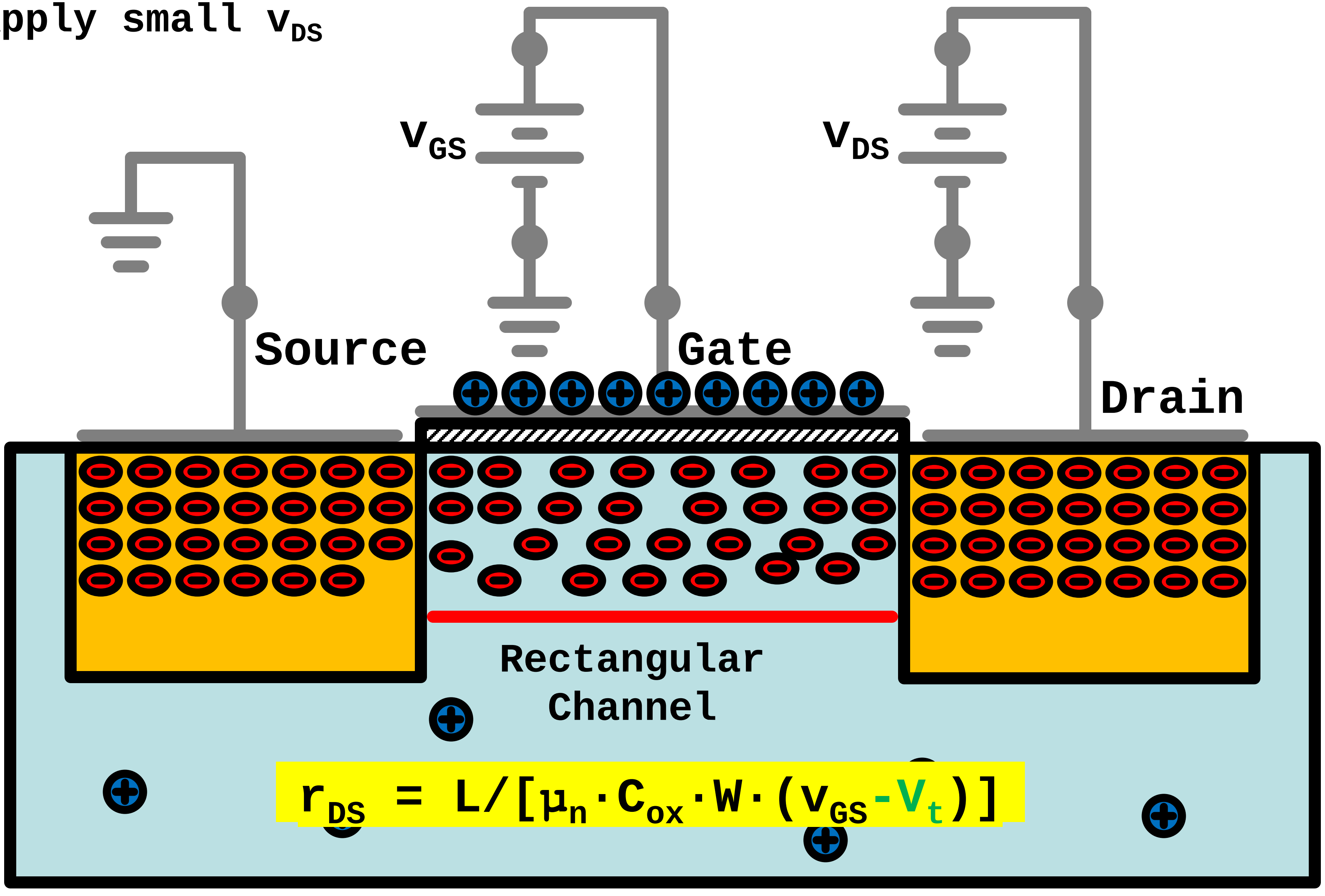
MOSFET – Operation and Modes

Increase v_{GS}
r_{DS} Decreases

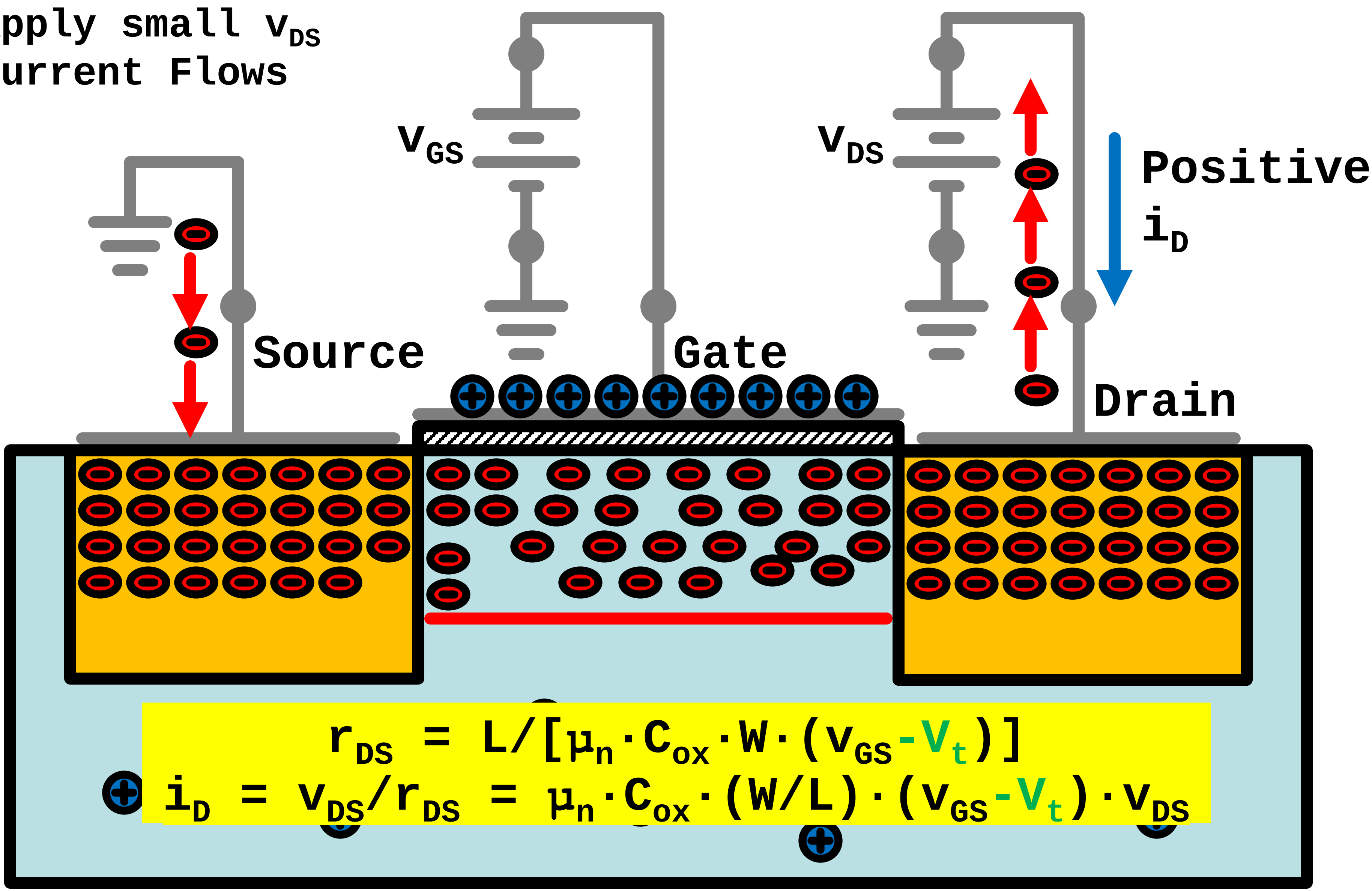


MOSFET – Operation and Modes

Apply small v_{DS}



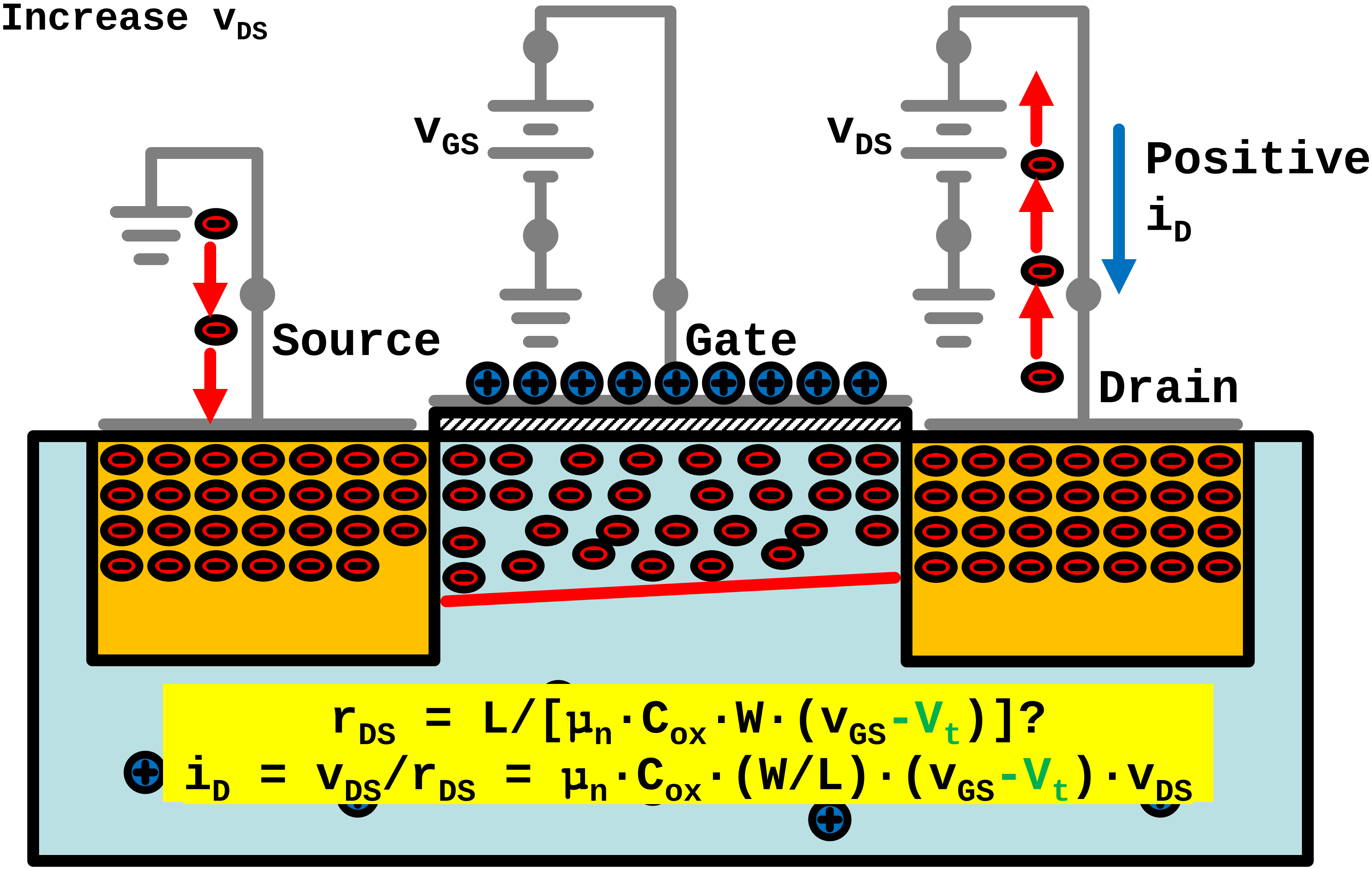
MOSFET – Operation and Modes



$$r_{DS} = L/[\mu_n \cdot C_{ox} \cdot W \cdot (v_{GS} - V_t)]$$

$$i_D = v_{DS}/r_{DS} = \mu_n \cdot C_{ox} \cdot (W/L) \cdot (v_{GS} - V_t) \cdot v_{DS}$$

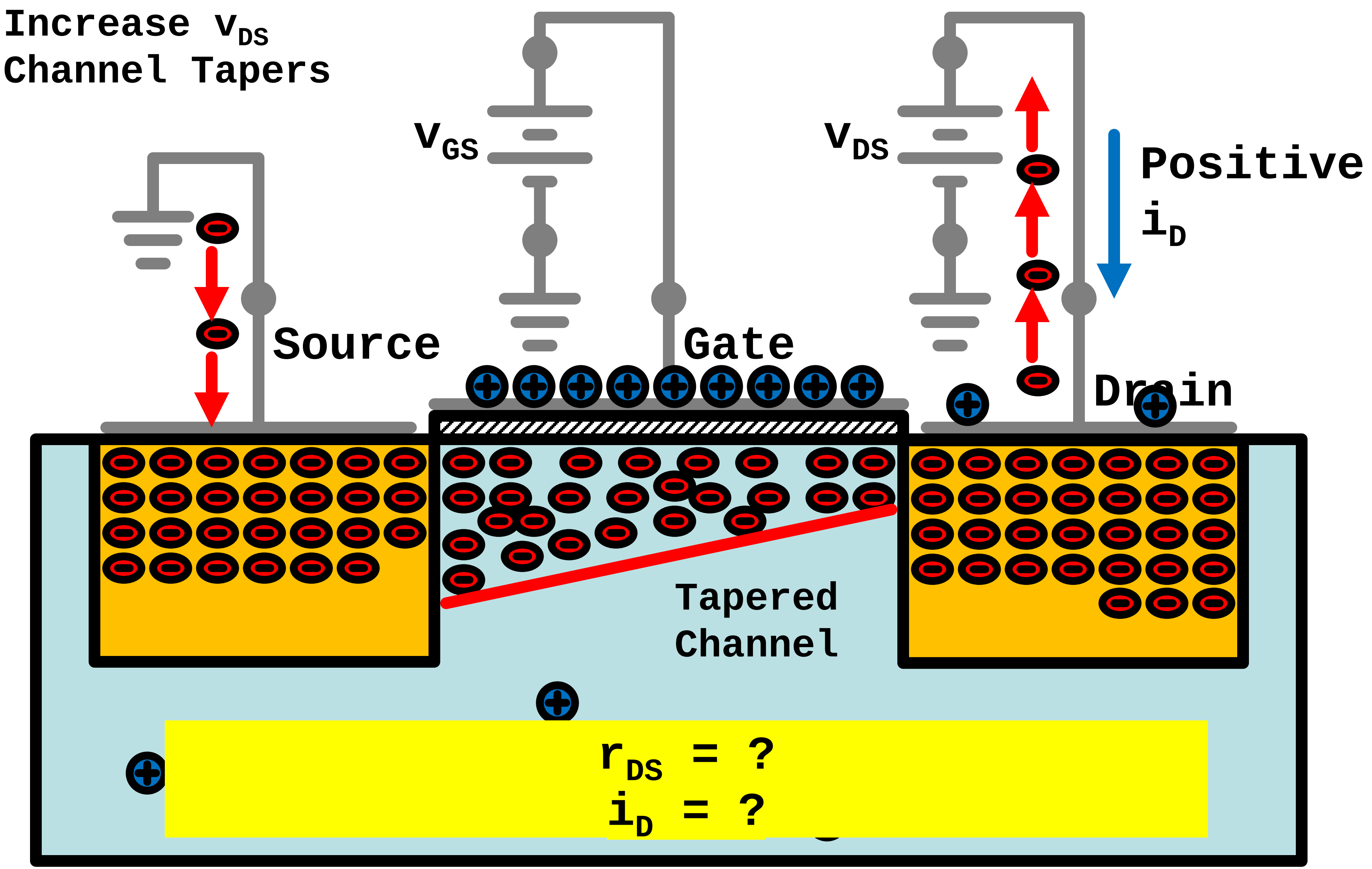
MOSFET – Operation and Modes



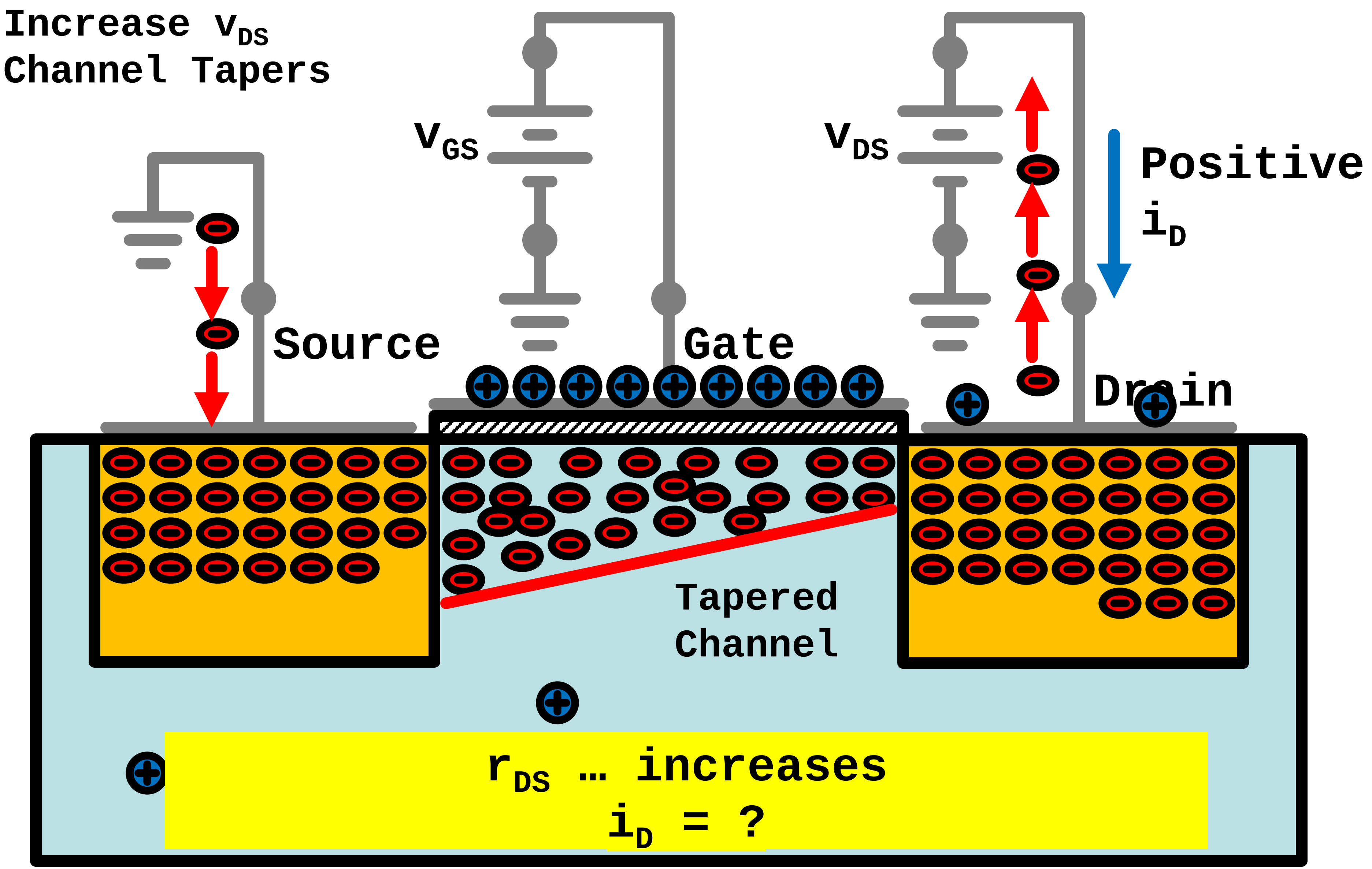
$$r_{DS} = L/[\mu_n \cdot C_{ox} \cdot W \cdot (v_{GS} - V_t)]?$$

$$i_D = v_{DS}/r_{DS} = \mu_n \cdot C_{ox} \cdot (W/L) \cdot (v_{GS} - V_t) \cdot v_{DS}$$

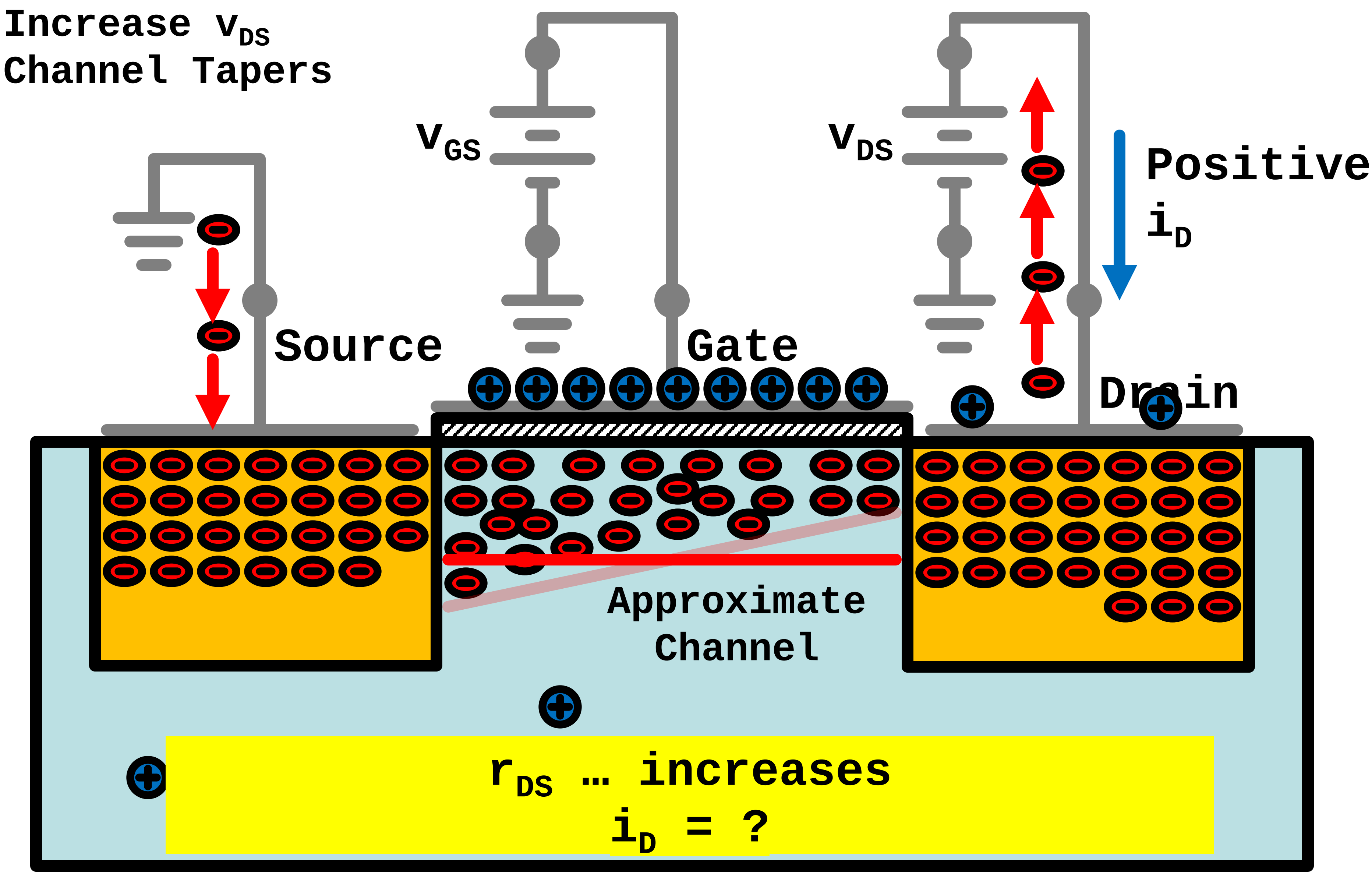
MOSFET – Operation and Modes



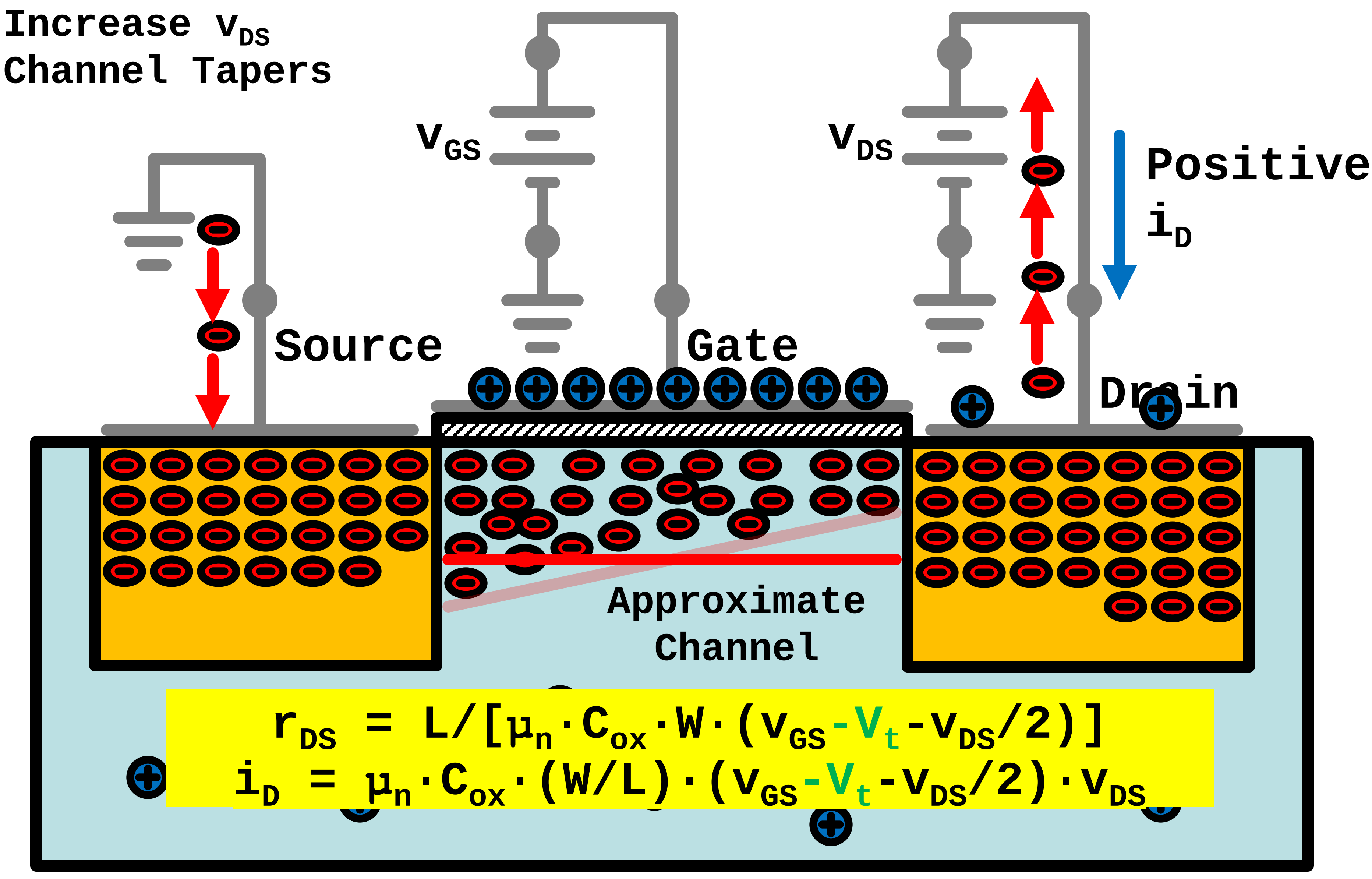
MOSFET – Operation and Modes



MOSFET – Operation and Modes



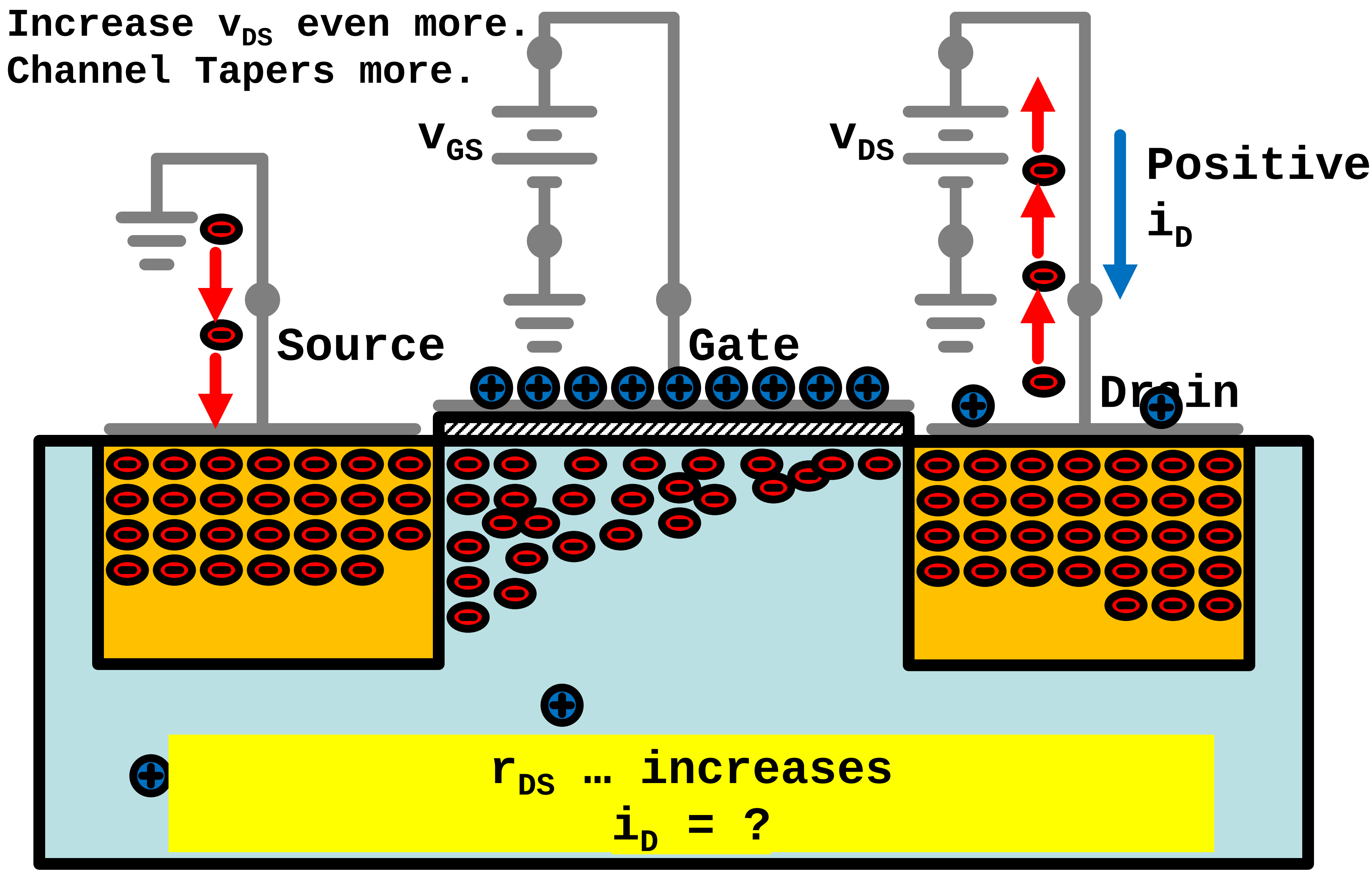
MOSFET – Operation and Modes



$$r_{DS} = L/[\mu_n \cdot C_{ox} \cdot W \cdot (v_{GS} - V_t - v_{DS}/2)]$$

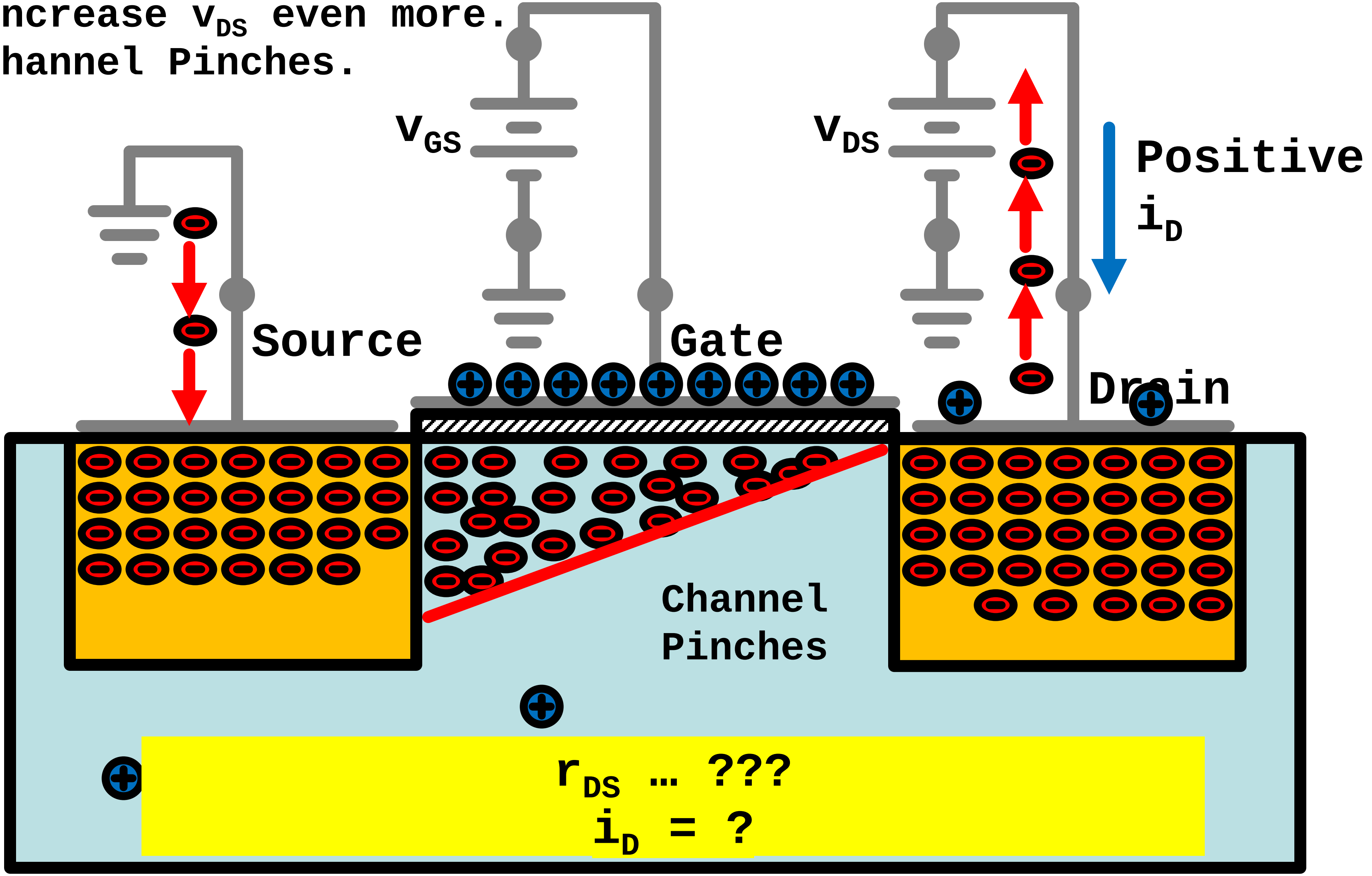
$$i_D = \mu_n \cdot C_{ox} \cdot (W/L) \cdot (v_{GS} - V_t - v_{DS}/2) \cdot v_{DS}$$

MOSFET – Operation and Modes



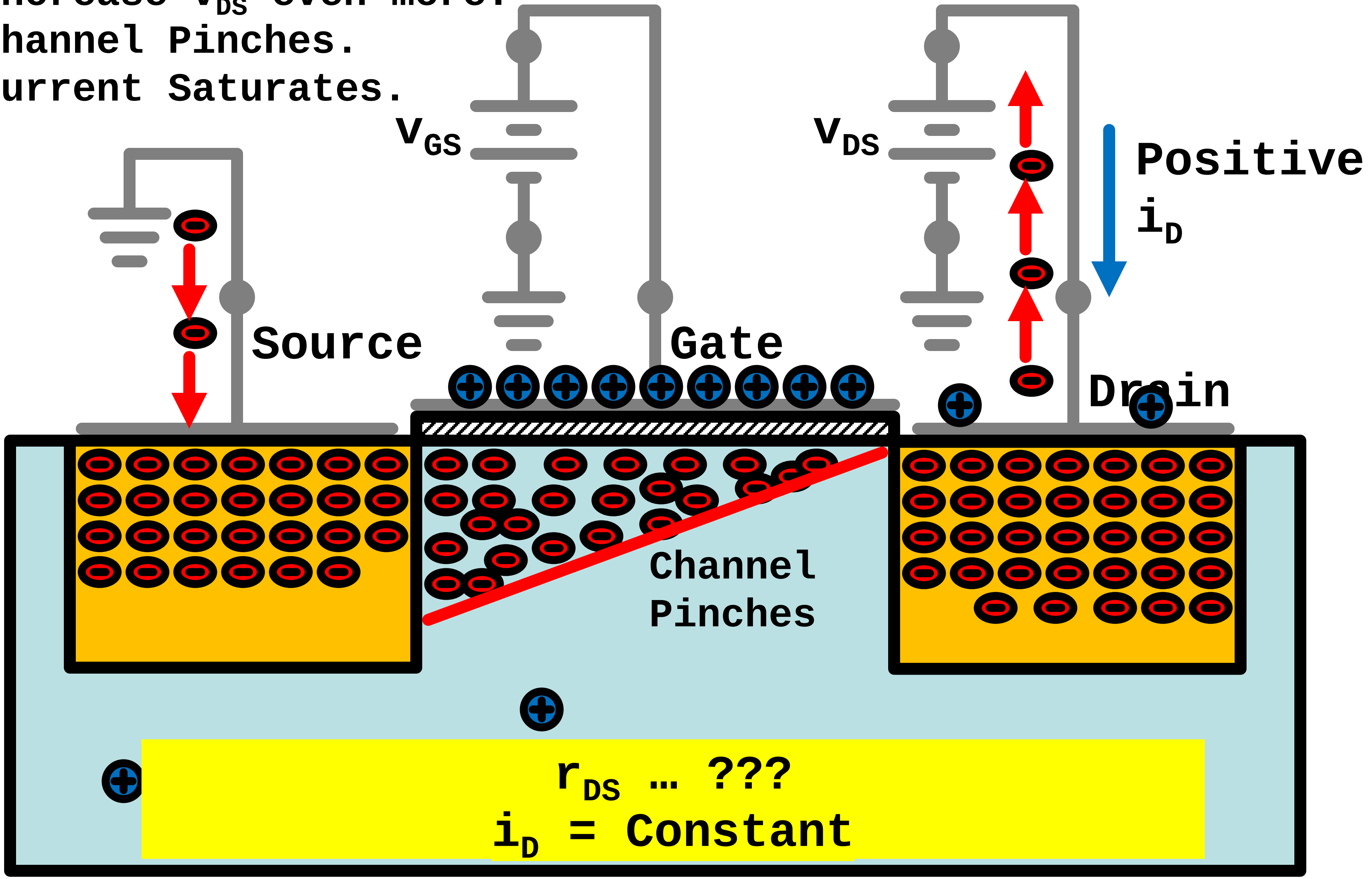
MOSFET – Operation and Modes

Increase v_{DS} even more.
Channel Pinches.



MOSFET – Operation and Modes

Increase v_{DS} even more.
Channel Pinches.
Current Saturates.



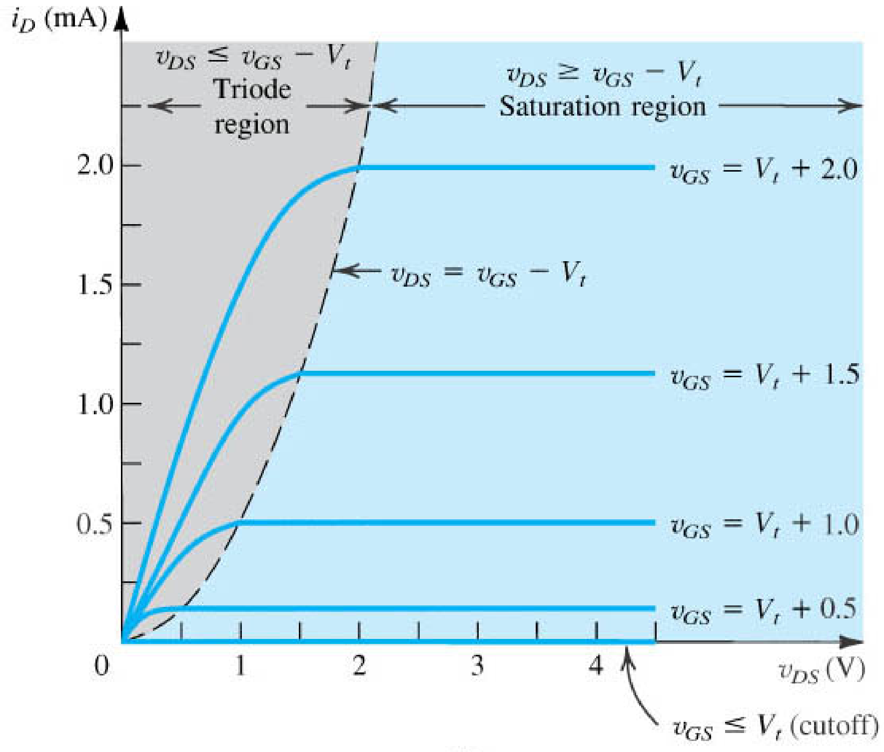
MOSFETs: Mode Dependence

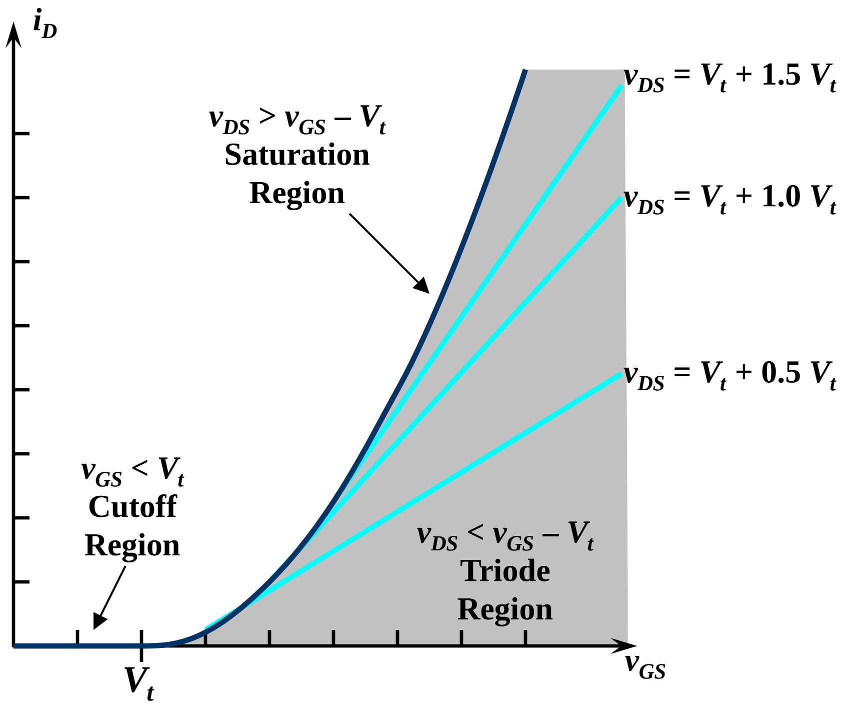
$$i_D = 0 \quad \text{for} \quad v_{GS} - V_t < 0 \quad \text{(cutoff)}$$

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS}\right] \quad \text{for} \quad v_{GS} - V_t > 0 \quad (\text{Triode}, v_{DS} << v_{GS} - V_t)$$

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{for} \quad v_{GS} - V_t > 0 \quad (\text{Triode}, v_{DS} < v_{GS} - V_t)$$

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[\frac{1}{2}(v_{GS} - V_t)^2\right] \quad \text{for} \quad v_{GS} - V_t > 0 \quad (\text{Saturation}, v_{DS} > v_{GS} - V_t)$$





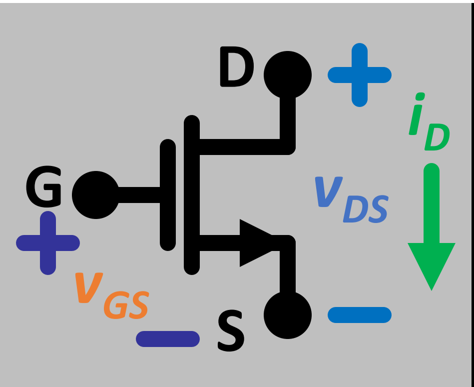
NMOS: Equations and Models

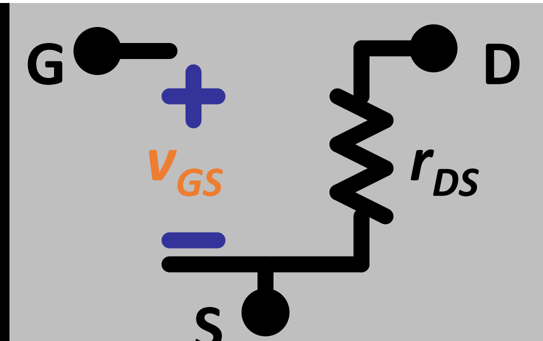
Mode	i-v Characteristic	Inequality Conditions	Channel Shape
Cut-off	$i_D = 0$	$v_{GS} - V_{tn} < 0$	No Channel
Triode	$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(v_{GS} - V_{tn} - \frac{1}{2}v_{DS}\right)v_{DS}$	$v_{GS} - V_{tn} > 0$ $v_{DS} < v_{GS} - V_{tn}$	Tapered
Triode (small v_{DS})	$i_D = \frac{v_{DS}}{r_{DS}} = \mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{tn})v_{DS}$	$v_{GS} - V_{tn} > 0$ $v_{DS} \ll v_{GS} - V_{tn}$	Rectangular
Saturation*	$i_D = I_D' = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$	$v_{GS} - V_{tn} > 0$ $v_{DS} \geq v_{GS} - V_{tn}$	Pinched
Saturation with Finite Output Resistance	$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2(1 + \lambda v_{DS})$	$v_{GS} - V_{tn} > 0$ $v_{DS} \geq v_{GS} - V_{tn}$	Pinched

$v_{GS} = v_G - v_S$
$v_{DS} = v_D - v_S$
i_D : Drain Current
V_{tn} : Threshold Voltage, $V_{tn} > 0$
$v_{OV} = v_{GS} - V_{tn}$: Excess Gate Voltage

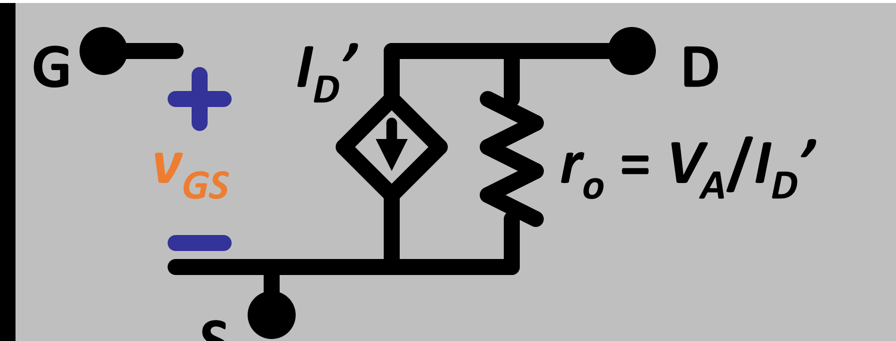
μ_n : Free Electron Mobility
$C_{ox} = \varepsilon_{ox}/t_{ox}$: Capacitance/Area
ε_{ox} : Oxide Permittivity
t_{ox} : Oxide Thickness
$k_n' = \mu_n C_{ox}$: Process Parameter

W: Channel Width
L: Channel Length
W/L: Aspect Ratio
$k_n = k_n'(W/L)$: Device Parameter
$V_A = 1/\lambda$: Early Voltage, $V_A > 0$





Triode (small v_{DS})



Saturation

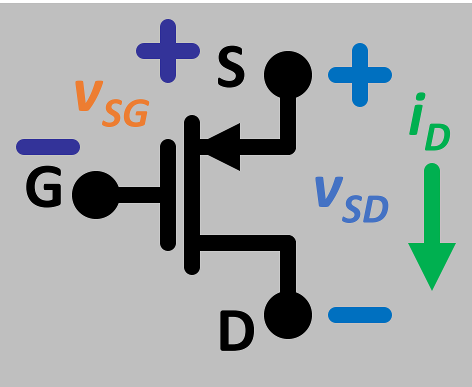
PMOS: Equations and Models

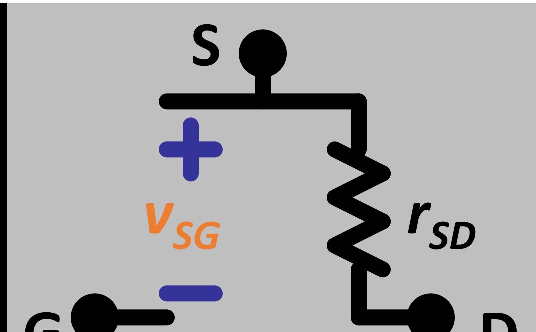
Mode	i-v Characteristic	Inequality Conditions	Channel Shape
Cut-off	$i_D = 0$	$v_{SG} - \lvert V_{tp} \rvert < 0$	No Channel
Triode	$i_D = \mu_p C_{ox}\left(\frac{W}{L}\right)\left(v_{SG} - \lvert V_{tp}\rvert - \frac{1}{2}v_{SD}\right)v_{SD}$	$v_{SG} - \lvert V_{tp} \rvert > 0$ $v_{SD} < v_{SG} - \lvert V_{tp} \rvert$	Tapered
Triode (small v_{SD})	$i_D = \frac{v_{SD}}{r_{SD}} = \mu_p C_{ox}\left(\frac{W}{L}\right)\left(v_{SG} - \lvert V_{tp}\rvert\right)v_{SD}$	$v_{SG} - \lvert V_{tp} \rvert > 0$ $v_{SD} \ll v_{SD} - \lvert V_{tp} \rvert$	Rectangular
Saturation*	$i_D = I_D' = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(v_{SG} - \lvert V_{tp}\rvert\right)^2$	$v_{SG} - \lvert V_{tp} \rvert > 0$ $v_{SD} \geq v_{SG} - \lvert V_{tp} \rvert$	Pinched
Saturation with Finite Output Resistance	$i_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(v_{SG} - \lvert V_{tp}\rvert\right)^2(1 + \lvert\lambda\rvert v_{SD})$	$v_{SG} - \lvert V_{tp} \rvert > 0$ $v_{SD} \geq v_{SG} - \lvert V_{tp} \rvert$	Pinched

$v_{SG} = v_S - v_G$
$v_{SD} = v_S - v_D$
i_D : Drain Current
V_{tp} : Threshold Voltage, $V_{tp} < 0$
$v_{OV} = v_{SG} - |V_{tp}|$: Excess Gate Voltage

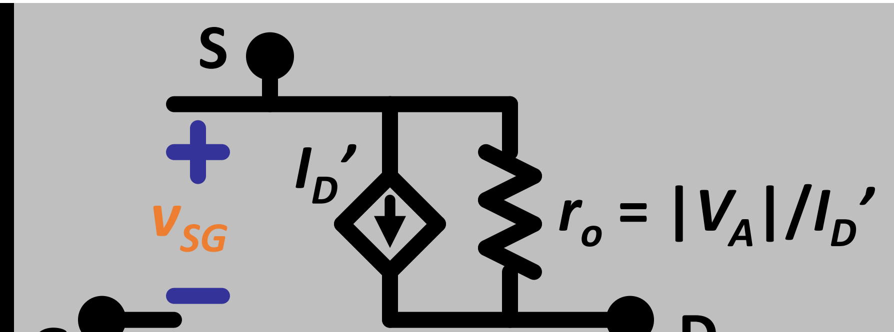
μ_p : Hole Mobility
$C_{ox} = \varepsilon_{ox}/t_{ox}$: Capacitance/Area
ε_{ox} : Oxide Permittivity
t_{ox} : Oxide Thickness
$k_p' = \mu_p C_{ox}$: Process Parameter

W: Channel Width
L: Channel Length
W/L: Aspect Ratio
$k_p = k_p'(W/L)$
$V_A = 1/\lambda$: Early Voltage, $V_A < 0$





Triode (small v_{SD})



Saturation

MOSFET Small Signal Model: Saturation Mode of Operation

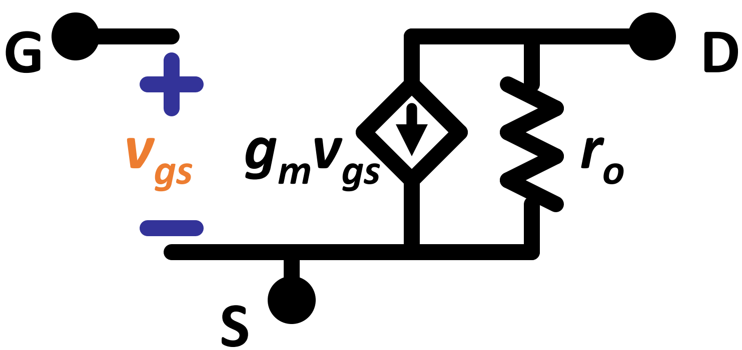
NMOS

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

$$g_m = \left.\frac{di_D}{dv_{GS}}\right|_{v_{GS}=V_{GS}} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})$$

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2(1 + \lambda v_{DS})$$

$$r_o = \left.\frac{dv_{DS}}{di_D}\right|_{i_D=I_D} = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$



PMOS

$$i_D = I_D' = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(v_{SG} - |V_{tp}|\right)^2$$

$$g_m = \left.\frac{di_D}{dv_{SG}}\right|_{v_{SG}=V_{SG}} = \mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{SG} - |V_{tp}|\right)$$

$$i_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(v_{SG} - |V_{tp}|\right)^2(1 + |\lambda| v_{SD})$$

$$r_o = \left.\frac{dv_{SD}}{di_D}\right|_{i_D=I_D} = \frac{1}{|\lambda| I_D} = \frac{|V_A|}{I_D}$$