Abstract

As the demand for high speed digital design circuits increases at the same rate as the required circuit sizes are decreasing, high speed design engineers need new solutions to overcome size restrictions. Using defected ground structures (DGS) to optimize the functionality of microstrip transmission lines is a newer method that capitalizes on the return current path characteristics that defects in the ground plane induce. This literature review brings the effectiveness of DGS configurations to microstrip transmission lines into light, and displays a case study example of how DGS circuits can be analyzed. DGS circuits could eventually become the key element that allows design engineers to design microstrip lines that are impervious to transmission leakage, while allowing them freedom to choose any line length they need to best fit their application.
Introduction

In high speed digital circuit design, the ground plane plays a vital role in the effective operations of the designed circuit. Without an adequately terminated ground plane, there would be a non ideal return path for the current to return to the source. Even with a properly terminated ground plane, there are other factors to be accounted for when designing a high speed digital circuit.

The return current path is a function of the electrical continuity of the ground plane. When an interruption in the ground plane occurs, such as a via or a slot, the current return path is lengthened. Figure 1 displays the current distribution on the ground plane when slots are present [4].

Figure 1: Current distribution on slotted ground plane [4]

This increased path length effectively increases the loop area, which in turn increases the effective inductance. Equation 1 represents the increased path inductance, where D is the entire slot length representing the deviation of the new current path from the original, and W is the trace of the width. Both are measured in inches.

\[ Ln \left( \frac{1}{D} \right) \text{ nH} \quad \text{Equation 1} \]

Recent research has attempted to capitalize on this increased effective inductance caused by lengthening the return current path. Research has concluded that increased effective inductance, and the subsequent increase in effective capacitance, caused by
interruptions in the ground plane will cause changes to the characteristics of planar transmission lines [1], [3]. The interruptions in the ground plane are commonly referred to as defected ground structures (DGS).

A DGS is an etched defect in the ground plane, beneath a planar transmission line [1]. DGSs can be both non-periodic which is referred to as DGS unit or periodic, depending upon its application. There are various DGS geometries, and each have many papers written about them with a wide range of applications. Figure 2 displays a few of the possible DGS configurations [1].

![Various DGS configurations](image)

Figure 2: Various DGSs: a. spiral head, b. arrowhead-slot, c. "H" shaped slots, d. a square open-loop with a slot in middle section, e. open-loop dumbbell, f. interdigital DGS [1]

The DGS can be modeled with an LC equivalent circuit. To do so the DGS must first have a computer simulation, and then its S-parameters must be extracted. From the extracted S-parameters a mathematical model using a one-pole Butterworth low pass filter (LPF) design can be used to represent the behavior of the DGS.

![LC Equivalent Circuit](image)

Figure 3: LC Equivalent Circuit: a. DGS LC Equivalent, b. Butterworth one-pole prototype low pass filter [1]
The LC equivalent circuit depicted in Figure 3.a is how the DGS is modeled. The series inductance \( L \) is a result of the return current path being elongated by the defect in the ground plane. The return current that flows at the edge of the DGS induces the effective series inductance. The parallel capacitor \( C \) represents the voltage gradients that exist between the gaps in the DGS. The DGS spacing acts as a capacitor and is represented in the equivalent circuit by a parallel capacitor \([2]\). The reactance \( X_{LC} \) of the equivalent DGS inductor and capacitor in parallel must be equal to the to the Butterworth LPFs cutoff frequency to correctly model the DGS \([1]\).

\[
\left( - \quad - \right), \Omega \\
\text{Equation 2}
\]

The Butterworth’s cutoff frequency is noted in Equation 2, where \( \omega_o \) is the resonance angular frequency. From Equation 2 the values of the equivalent inductor and capacitor values can be calculated \([3]\).

\[
\frac{1}{\pi f^2}, \text{F} \\
\text{Equation 3}
\]

\[
\text{H} \\
\text{Equation 4}
\]

In Equations 3 and 4 \( f_c \) is the cutoff frequency, \( f_o \) is the resonant frequency and \( Z_O \) is the characteristic impedance from figure 3.a \([3]\).

Despite using ideal high speed circuit design techniques, microstrip lines are still subject to spurious signals and leakage transmission. These issues can be minimized by using DGSs. One advantage to the DGS structure is its stop band effects. The nature of the DGS induced inductance results in frequency dependent and designable stop band rejection. This application of DGSs has spawned an entire avenue of research using DGSs as microwave filters \([1]\).

Another advantage of DGS structures are its slow-wave effects. The length of a microstrip line is a function of the dielectric constant of the substrate that it’s mounted on. Therefore, once the substrate is chosen, there isn’t much a design engineer can do to alter the phase velocity, so the length of transmission line fixed. The slow-wave effect shortens the
wavelength in the transmission line. This is accomplished by taking into account the increased
induced effective inductance and how it relates to the phase velocity of the signal in the
transmission line. Equation 5 shows how phase velocity ($V_p$) is related to the equivalent
inductance ($L_{EQ}$) in a microstrip line.

$$\sqrt{\frac{1}{k}} \text{ in / ps} \quad \text{Equation 5}$$

As the perimeter of the DGS increases, and DGS spacing is maintained so the capacitance is
unaltered, the effective inductance caused by the DGS increases, which reduced the phase
velocity. A reduced phase velocity allows for the transmission line to be shorter, and therefore
the overall circuit dimensions can be smaller as well [5].

The main disadvantage to using a DGS design, is the lack of correlation between the
dimensions of the DGS and its equivalent LC circuit parameters. The equivalent LC circuit
parameters can only be obtained after the circuit has been simulated, and having obtained the
S-Parameters. The optimal, and possibly not the best, design is only realized after numerous
iterations, and various DGS dimensions have been simulated and their S-Parameters have
been extracted [1].

Interpretation and Application

Using high speed circuit design analysis for measuring the effective inductance of a
ground plane interruption, Equation 1, a case study was done on some of results that were
obtained in [3]. In the paper, the effective inductance and capacitance were not explicitly
measured, however their frequency response was extracted by S-parameters obtained through
the simulation software Ansoft HFSS 13.0. From this an LC equivalent circuit could be
modeled. The DGS used in their report was a circular DGS which is depicted in figure 4.
Using the DGS parameters as specified in the paper, the effective inductance, effective capacitance and cutoff frequency could be calculated. The first design of paper simulated had the values found in table 1.

Table 1: Circular DGS Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microstrip Impedance</td>
<td>40 Ω</td>
</tr>
<tr>
<td>Microstrip Width (W)</td>
<td>1.79 mm = 70.4 mils</td>
</tr>
<tr>
<td>Microstrip Length (L)</td>
<td>21.03 mm = 828 mils</td>
</tr>
<tr>
<td>Dielectric Constant of Substrate</td>
<td>2.5</td>
</tr>
<tr>
<td>Thickness</td>
<td>0.635 mm = 25 mils</td>
</tr>
<tr>
<td>Original Operating Frequency</td>
<td>2.31 GHz</td>
</tr>
<tr>
<td>Radius of Circle</td>
<td>3.74 mm = 147.2 mils</td>
</tr>
<tr>
<td>Gap Length</td>
<td>0.1 mm = 4 mils</td>
</tr>
<tr>
<td>Total (D)</td>
<td>15.06 mm = 593 mils</td>
</tr>
</tbody>
</table>

$$L = \frac{1}{\pi f_0} \ln \left( \frac{2D}{d} \right) \text{ nH}$$

$$L = 6.318 \text{ nH}$$

Using Equation 1 the effective inductance caused by this circular DGS configuration was calculated to be 6.314 nH. When the structure was simulated, in the paper with the DGS the
resonant frequency changed from its original 2.31 GHz without the DGS, to 1.53 GHz with the DGS. Using the new 1.53 GHz resonant frequency, Equation 4 can be utilized to realize the effective capacitance.

\[ C = 1.7123 \text{ pF} \]

With the effective inductance and capacitance values obtained, Equation 3 can be used to calculate the cutoff frequency of the equivalent circuit.

\[ f_c = \frac{1}{\pi \sqrt{L_C C}} \]

\[ f_c = 1.06 \text{ GHz} \]

The equivalent LC circuit for the specific test configuration noted in table 1 can be seen in Figure 5.

![Figure 5: Case Study Equivalent LC Circuit](image)

Thought paper didn’t specify the equivalent LC circuit parameters, the values were able to be extracted using high speed circuit design techniques paired with a few equations obtained from various papers.
Conclusion

The paper [3] in which this literature review does a case study on, went on further to test and verify the effects on the LC circuit equivalent as various parameters. The first test was to vary the physical dimensions of the DGS and observe its effect on the circuit, while the gap distance $g$, the substrate material and the width of the transmission line were all held constant. As the radius of the two circles was increased, both the resonant and cutoff frequencies decreased. This is expected because as the radius increases, the return current path elongates, which causes the effective inductance to increase, which is inversely proportional to both the cutoff and resonant frequencies. The second test was to keep the radius of the circles constant and only vary the gap distance. As the gap distance was varied the resonant frequency decreased, and the cutoff frequency remained unchanged. From these results, as well as Equations 3 and 4, it can be concluded that the equivalent series inductance is a function of the physical dimensions of the DGS, while the equivalent parallel capacitance is a function of the gap distance [3].

The tests from paper [3] confirmed the expected results from the researched knowledge acquired on DGS behaviors. They displayed how the inductance is a function of current deviation, the capacitance is a function of gap distance, and how the resonant and cut off frequency of the various configurations are functions of the DGS dimensions.

When using microstrip lines for high speed digital circuit design, in conjunction with a possible RF operations, DGS structures can be used to minimize transmission leakage. The demand for high speed circuits that can transmit and receive data is always increasing, while the device size is decreasing. DGSs offer designers the ability to put protective measures on their transmission lines by altering the ground plane they’re mounted on. Along with these compact configuration, the other layer of protection is having shorter transmission lines which the DGSs also offer. One DGS under one transmission line can offer a slower phase delay on the line, allowing for a smaller run, as well as stop band rejections of a nearby oscillating frequency. Both of these benefits assist the high speed digital circuit designer in their design process.

Further research in the area of defected ground structures is required to enhance its mathematical model, which would in turn increase its optimization of high speed circuit design applications. With the overall benefit DGSs bring to the high speed digital design, it’s only a matter of time before etched ground planes are common practice amongst design engineers.
References


