This reading is taken from *CMOS Cookbook*, by Don Lancaster. It contains some important hints on using the 4046 PLL

The 4046

The 4046 has two separate internal circuits. One is a vco that runs from subaudio frequencies to beyond 1 MHz. The other is a dual-output phase detector. To this, you add a divide-by-n counter (or a jumper for n = 1) and a two-resistor, one-capacitor loop filter in order to build a complete phase-locked loop.

We have already learned about the vco portion of the 4046 back in Chapter 4. The center frequency range is set by a capacitor on pins 6 and 7. The maximum frequency is set by a 10K to 10-megohm resistor connected from pin 11 to ground; any frequency offset is provided by a usually larger resistor connected from pin 12 to ground. A voltage input to pin 9 will sweep the frequency between the limits set by the two resistors. Ground gives you a minimum frequency, and +V gives you the maximum frequency. This is a typical high-impedance CMOS input that won't load the loop filter.

Rather than go into the complicated internal details of our dual phase detector, we will just summarize what each detector option does for you in Table 7-2. There is an input for an external reference on pin 14, and an input for the divide-by-n on pin 3. Note that these two pins cannot be interchanged because it will reverse the sense of the loop. If n is going to be 1, you simply jump the pin 4 vco output to pin 3; if n comes from a counter, the vco output clocks the counter, and the counter output drives pin 3.

There is a choice of two phase-detector outputs. One is a conventional (EXCLUSIVE OR) or *low-noise* phase detector; the other is the new-to-CMOS *wideband* phase detector.

The low-noise phase-detector output on pin 2 has a limited tracking range that is hard to get beyond ±30 percent, but it provides

Table 7-2. Comparison of Wideband Phase Detector and Low-Noise Phase Detector, Both Using a 4046 PLL

Wideband Phase Detector	Low-Noise Phase Detector
Outputs on pin 13	Outputs on pin 2
Tracks over very wide frequency range, to 2000:1 if needed	Maximum tracking range is ±30%
Noise immunity is limited	Excellent noise immunity
Input signal can be narrow pulse or other duty cycle	Input signal must be a square wave
With no input, output frequency goes to lowest designed value	With no input, output frequency goes halfway between high and low limits
Output phase is 0° with respect to input	Output phase is 90° for midfrequency input, varies with frequency
Insensitive to harmonics	Harmonic sensitive
Loop filter acts as sample-and-hold	Loop filter acts as integrator

very good noise rejection. *For this phase detector to work, both input signals must be 50/50 duty-cycle square waves.* You use this phase detector when replacing traditional analog PLLs with the 4046. The output phase of your vco will be roughly 90° for midband input frequencies and will increase or decrease as your input reference frequency changes.

The wideband phase detector is actually a digital-logic phase/frequency detector. It provides a tri-state sample-and-hold output on pin 13 for the loop filter. If the input *frequency* is higher than the vco, a steady high output results. If the input frequency is lower than the vco frequency, a steady low output results. If the two frequencies are identical, the phase detector outputs a pulse proportional to the phase difference. This pulse is positive going for lagging vco phase and is negative going for leading vco phase.

The input frequency can range over an extremely wide area, even beyond 1000:1 if desired, and the vco phase is always 0° with respect to the input frequency when locked. The input and reference frequencies can be any duty cycle from a square wave down to narrow pulses of either polarity. This detector is the best choice for most newer PLL designs, particularly those that have to operate over a wider frequency range. The noise-rejection characteristics of this wideband detector are generally poorer than those of the low-noise phase detector; this is about its only real disadvantage.

A separate "test-phase" output that may be used for lock detection with either detector is available on pin 1. The input to either phase detector is pin 14. This input will, in theory, accept capacitively coupled low-level signals and amplify them to digital logic levels, or it can be driven directly by CMOS logic that swamps the internal amplifier.

The linear amplifier operation of pin 14 is an unmitigated disaster when the wideband phase detector is being driven. Don't use it this way! Linear operation causes extra amplitude-variation sensitivity, jitter, tearing, and generally poor noise immunity. Instead, drive your input with a full logic signal or use a resistor to pull it over to one extreme supply limit and capacitively couple an input signal. If your input signal is very small, amplify and limit it externally, particularly for low-frequency references such as the power line.

Loop Design

To get your phase-locked loop to work, you have to add a *loop filter* to it. All this takes is two resistors and a capacitor. While deceptively simple, the loop filter is the single most important part of any PLL. Figure 7-20 gives some details on loop-filter design.

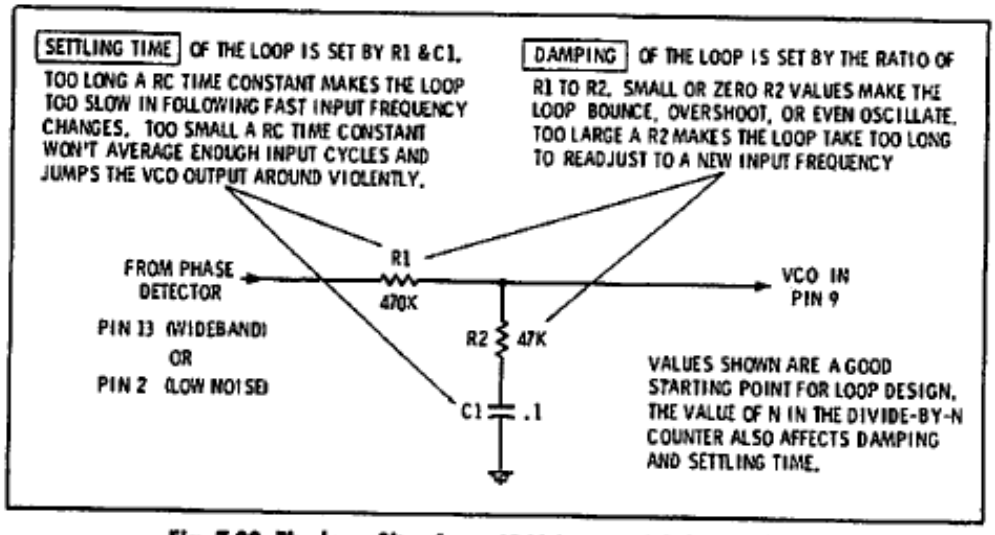

Fig. 7-20. The loop filter for a 4046 is a crucial design detail.

The loop filter decides two things for us—the *settling time*, or how many cycles the loop is going to average, and the *damping*, or the ability of the loop to accept new changes without excessive overshoot or possible oscillation. If the PLL was a pendulum, the settling time would be decided by the mass and length of the arm; the damping would be determined by air resistance and the friction of the pivot.

Generally, the low-noise phase detector takes a much longer settling time than the wideband detector since the capacitor is a continuously driven integrator or averaging device, while the wideband detector uses the capacitor as a sample-and-hold that is difference driven. Also, you will probably want long settling times when n in the divide-by-n counter is large. This prevents the early vco output

from being different than the later vco output *for each cycle of phase-detector operation.*

It may seem that the "smoothest" loop operation would be gained by omitting R2 so that the capacitor directly "filters" the vco input. However, this is not so! Omitting R2 will almost always drive the loop into near oscillation, causing extreme underdamping and taking a long time rebounding in a damped oscillatory manner. The math behind this is detailed in *Phaselock Techniques* by Floyd M. Gardner, but the important point for us is that we will get the best loop operation with a series resistor, typically one-tenth to one-third the input resistance.

The actual loop design isn't really difficult. You should use the longest possible settling time you can. Generally, you start with the values given in Fig. 7-20 and close the loop. Then you produce a sudden change in input frequency near the lower limits of intended vco operation, and watch the output frequency or the vco control voltage on a scope. The quickest operation is obtained when you let the vco overshoot around 40 percent on a step error. This is near *critical damping.* If you don't want overshoot, use correspondingly higher R2 values to increase the damping.

After you have some values that look reasonable, check the vco output for steady-state jitter. With high values of n, more settling time may be needed to keep the vco sweeping back and forth during each cycle of phase-detector comparison. This is particularly important if you are using the low-noise phase detector. Let's clear up some of these PLL mysteries with some design examples.