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A Graph Topology Independent Method of Evaluating the Detection Probability Distribution of A VLSI Circuit

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Abstract

The problem of test set generation of a combinational circuit is known to be NP-complete for circuits with general graph topology. The detection probability distribution of a given circuit is known to aid in the test generation process. In this paper we present a new method of evaluating the detection probability distribution *of a circuit. We use a relation we developed to propose a* graph topology independent *method of evaluating such a distribution. The distribution is modeled as a series of impulse functions with strengths evaluated from fault coverage data. Existing algorithms are dependent on the graph topology of a circuit. These methods use simplifying assumptions to offset the computational overhead. Experimental results given on three of the large ISCAS benchmark circuits reflect the accuracy of our method.*

Key Words: Detection Probability, Detection Probability Distribution, Fault Coverage, Fault Simulation.

1 Introduction

The test set generation problem is to find a subset of the input space of a proposed digital design that detects a set of modeled faults [6, 9, 10]. This problem is known to be NP-complete [7]. The Detection Probability Distribution of a circuit is assumed to aid in the design process of VLSI chips by providing analytic measures of the "ease" or "difficulty" of generating test sets. These measures can be used to isolate certain portions of a proposed design before it becomes a physical reality. The portions isolated, those that are considered hard to test, could then undergo possible design improvements.

Several algorithms evaluating the detection probability distribution exist [8, 11] where a combinational circuit is modeled as a directed graph and the detection probability distribution is graph topology dependent. The computational complexities of existing algorithms vary from linear to exponential in the size of the circuit, depending on the level of accuracy desired.

In [1, 12] we have established a relationship between *fault coverage* of test sets (generated deterministically [6] or undeterministically), and the detection probability distribution of a circuit. Using this relation, we proposed a

new method of test generation by tailoring the standard test generation process to a sample of faults. The sample size as well as the detection probability distribution were estimated during what we called "pass one." Our estimates, however, used Bayes theorem with *uniform* apriory detection probabilities, and were biased to special *unknown distribution* of input vectors.

In this paper we propose a new procedure of evaluating the detection probability distribution of a circuit that is independent from its graph model. The apriory distribution of the detection probability distribution is assumed to be a set of *impulse functions of varying strengths.* The accuracy of the method is a function of the number of impulse functions used. The strength of the modeled impulse functions are evaluated from fault coverage data computed during a normal course of test generation restricted to a sample of faults. We apply our method on three of the large ISCAS [4] circuits, C2670, C6288, and C7552, and use the statistical package Minitab to measure the accuracy of our method.

Applications of our analysis include: determining the size of a test needed to yield a certain fault coverage without fault simulation, extrapolation of fault coverage of a set of vectors from partial fault coverage, and test generation by fault sampling.

The paper is presented as follows. In section 2, we give the needed definitions and present the graph model of a combinational circuit. Section 3, contains background material and an example of a graph topology dependent method of evaluating the detection probability distribution. Section 4 includes the determination of fault coverage from known detection probability distributions. Section 5 includes modeling the detection probability distribution as a series of impulse functions and evaluating the parametes of the model from fault coverage data. In section 6, we present our experimental results on three of the large ISCAS circuits and evaluate the statistical bounds on the computed parameters using Minitab. The results are summarized in the conclusion in section 7.

2 Definitions and the Graph Model

A line or a gate is said to be *stuck at zero (one)*, written as *s-a-0 (s-a-1)*, if it permanently assumes a value of zero (one). The *fault population (FP)* of a circuit is composed of all single s-a-0 and s-a-1 faults. The set of all possible inputs will be represented by I^n, where n is the number of input pins to the circuit under test and $I = \{0, 1\}$. The set of all possible outputs will be represented by O^m, where m is the number of output lines and $O = I$. For a given combinational circuit C and a given fault α, we say that α is irredundant if and only if there exits an input sequence that will yield different responses in the presence and absence of fault α, otherwise α is called redundant.

A Boolean function F realized by a circuit C with n inputs and m outputs can be modeled by a mapping function $F : I^n \rightarrow O^m$, and is written as: $F = (f_1, f_2, \ldots, f_m)$. Similarly, $F_\alpha = (f_{1\alpha}, f_{2\alpha}, \ldots, f_{m\alpha})$ will

be used to denote the output function of the circuit C in the presense of the fault α. Formally, a fault α is called *an irredundant fault* if there exists an input vector $(i_1, i_2, \ldots, i_n) \in I^n$ and j, $j \in \{1, 2, ..., m\}$, such that $f_j(i_1, i_2, \ldots, i_n) \neq f_{j\alpha}(i_1, i_2, \ldots, i_n)$.

Such input vector $(i_1, i_2, \ldots, i_n)$ is called a test for the fault α. If there exists no such input vector for α, α is called *a redundant fault.*

If $T(\alpha) = \{t \in I^n : t \text{ is a test for fault } \alpha\}$, then $T(\alpha)$ is called the test set for α.

A line i is said to be a *fan-out node* (stem) if several lines in the circuit converge at i. The convergent lines are called the *fan-out branches* of i. We call i a *reconvergent* fan-out node if at least two of its corresponding branches reconverge as inputs to some gate. A circuit is said to have a tree structure

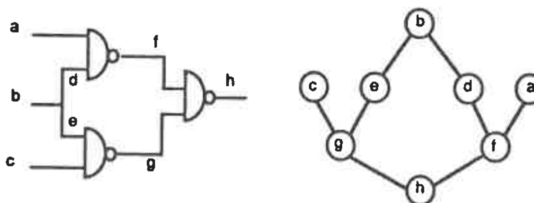

Figure 1: A Combinational Circuit and its Graph Model

if it does not contain any fan-out nodes.

Any combinational circuit C can be represented by a directed graph $G_C = (V, E)$. The graph can be constructed as follows. The set of vertices, V, corresponds to the lines in the circuit C, and a directed edge $(u, v) \in E$ if and only if the line corresponding to vertex u is an input to a gate for which the line v is the output, or the line v is a fan-out branch of the fan-out node u. An example of a combinational circuit and its graph representation is shown in Fig. 1. The direction of the edges is eliminated in the figure since the direction of all edges is assumed to be top down.

This representation will be complete if all the gates in the circuit are the same. In the case of circuits with different gates, a code can be associated with each vertex, v, to indicate the type of gate to which the line v is the output.

We associate with each node of the graph of a combinational circuit two *detection probability* values corresponding to the two possible single-stuck-at failures of the node. Formally, the detection probability of a fault α (x_α) is defined as the probability of detecting α by a random input and is given as

$$x_\alpha = \frac{|T(\alpha)|}{|I^n|}.$$

The *detection probability distribution* (henceforth denoted as $p(x)$) of a combinational circuit is the probability density function of the detection probabilities of its faults. Since $p(x)$ is probability density function we have

$$\int_0^1 p(x)\, dx = 1.$$

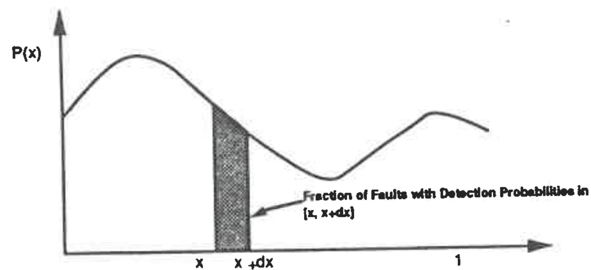

Figure 2: Arbitrary p(x) distribution

Fig. 2 shows the distribution of $p(x)$ of an arbitrary combinational circuit.

Note that in the figure $p(x)dx$ corresponds to the fraction of detectable faults with probability of detection between x and $x + dx$.

Fig. 3 shows the $p(x)$ distribution obtained from simulating the effect of all single-stuck-at failures on the graph model in Fig. 1. A test for a fault α causes the response monitored at the output node (node h) of the graph to differ from the expected response. Since the graph model of the combinational circuit contains eight nodes the number of faults is 16 (two failures are associated with each node).

The distribution of $p(x)$ for a given circuit can be determined to various levels of accuracy using different algorithms like PREDICT [11] and COP [3].

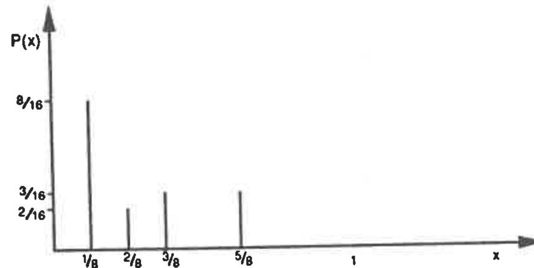

Figure 3: Computed p(x)

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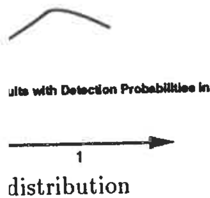

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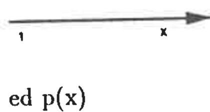

ed p(x)

Let $T \subseteq I^n$ such that $|T| = k$. The *fault coverage* y_k by T is defined as

$$y_k = \frac{\sum_{\alpha \in FP} \ \alpha_i}{|FP|}$$

such that $T(\alpha_i) \cap T \neq \emptyset$. That is, the fault coverage y_k is defined as the fraction of faults detected by inputs taken from T.

3 Detection Probability Distribution and Fault Coverage

This section contains some of the background material needed in the paper. We briefly summarize some of our results in the form of two theorems without proofs; the interested reader may refer to [1, 12]. In addition (for comparison purposes with the proposed method), we present a graph topology dependent algorithm , PREDICT, for evaluating $p(x)$.

Probablistic Estimation of Digital Circuit Testability (PREDICT) [11] is an algorithm that computes the testability of a circuit. It employs a graph theoretic approach to compute the exact detection probabability values of all modeled faults. We summarize the steps used by PREDICT below.

- The algorithm forms the graph model of the circuit C.
- From the graph model, it identifies all reconvergent fan-out nodes. Let $\{l_1, l_2, ..., l_k\}$ denote the set of all reconvergent fan-out nodes of C, and let $C = \{(c_1, c_2, ..., c_k)/c_i \in \{0, 1\}, i = 1, 2, ..., k\}$ be the set of all binary assignments to the fan-out nodes.
- The algorithm then uses the probability of setting a given node, l, to one to determine the detection probability distribution. The probabbility of setting node l to one is given as

  $$Prob(line\ l = 1) = \sum_{C} Prob(line\ l = 1/C) * Prob(C).$$

  Note that the computational time is linear if the circuits underlying graph is a tree graph (circuit contains no reconvergent fan-out nodes). However, for graphs with number of cycles exceeding the number of inputs the computations are exponential. To offset the exponenetial computational costs the algorithm computes approximate values of the detection probability of a node. Where, in a preporcessing step, the algorithm identifies (from among all the reconvergent nodes) those nodes that are at a distance x from l where x does not exceed some predefined value. The identified nodes are then used to estimate the detection probability of l.

  The method we present estimates the detection probability of modeled faults; however, unlike existing methods, the method is circuit topol-

ogy independent. Assume n random vectors are applied to a circuit with some known $p(x)$ distribution. The expected coverage by the first vector on faults with detection probability in $[x, x + dx]$ is $x\,p(x)\,dx$. The expected coverage by the first vector on all faults is

$$y_1 = \int_0^1 x\,p(x)\,dx$$

For n vectors we obtain the following theorem.

Theorem 1 *Let n be the number of random vectors applied to circuit C with known $p(x)$. Then, the expected random fault coverage, y_n, is*

$$y_n = 1 - \int_0^1 (1-x)^n\,p(x)\,dx$$

Note that the more the graph of $p(x)$ is skewed to the right the larger the coverage by a given set of inputs is expected. Fig. 4 shows two extreme cases of the distribution of $p(x)$. In Fig. 4 (a), $p(x)$ is modeled as an impulse function at $x = 0$. The distribution of $p(x)$ indicates that the detection probabilities of all faults in the circuit is zero. The expected coverage y_n, hence, should be zero for any value n. This is the case when the integral term in equation (1) is evaluated. Similarly, in Fig. 4 (b), the expected coverage y_n for any $n \geq 1$ is found to be 1.

For deterministic coverage, we assume that each newly generated vector detects at least one fault not detected by already generated tests. And, the newly generated vector acts as a random vector on the remaining

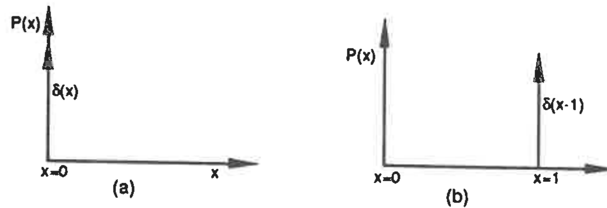

Figure 4: Two extreme distributions of p(x)

faults. This assumption is a direct consequence of how deterministic test generators work [6].

In the initial phase of test generation, it is usually true that the curves for random coverage and deterministic coverage are very similar. This can be seen by evaluating the deterministic coverage y_1. The deterministic coverage can be found as

$$y_1 = \frac{1}{FP} + \left(1 - \frac{1}{FP}\right) \int_0^1 x\,p(x)\,dx,$$

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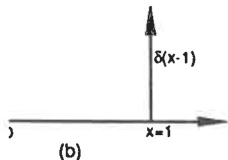

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$\frac{1}{FP}\Big) \int_0^1 x\, p(x)\,dx,$

where FP is the fault population associated with a given circuit.

Using the same analysis applied to random coverage, we obtain the following theorem.

Theorem 2 *Let C be a circuit with known $p(x)$ and let y_n be the deterministic fault coverage by n vectors. Then, the expected coverage is*

$$y_n = 1 - \int_0^1 (1-x)^n p(x)\,dx + \frac{n}{FP}\left[1 + \int_0^1 (1-x)^n p(x)\,dx - \int_0^1 \frac{1-(1-x)^n}{nx} p(x)\,dx\right].$$

Table 1: Coverage from Testability

Testability Profile	y_n
$p(x) = 1, 0 < x \leq 1$ (uniform)	$1 - \frac{1}{n+1}$
$p(x) = \delta(x - x_0)$ Impulse at $x = x_0$	$1 - e^{[ln(1-x_0)]n}$
$p(x) = \sum_{i=0}^{k} \alpha_i \delta(x - x_i)$ sum of Delta Functions	$(1-\alpha_0) - \sum_{i=1}^{k} \alpha_i e^{[ln(1-x_i)]n}$

4 Fault Coverage Prediction From Detection Probability Distribution

Table 1 shows a closed form solution for fault coverage derived from simple known forms of $p(x)$. The first row corresponds to an extreme case of a uniform distribution of $p(x)$ over the interval $[0, 1]$. For this case, the fraction of undetected faults is inversely proportional to n. In the second row, we have another extreme case of modeling $p(x)$ as an impulse function located at $x = x_0$. The coverage for the cases $x_0 = 0$ and $x_0 = 1$ were discussed earlier. For $x_0 = 0$ the coverage was found to be 0 for all $n > 0$; for $x_0 = 1$ the coverage is 1 for all $n > 0$.

The last case shown in the table is a series of impulse functions located at $x_0, x_1, \ldots, x_k$. Each impulse function at x_i has a strength of α_i such that

$$\textstyle\sum_{i=0}^{k} \alpha_i = 1, \text{ and } \alpha_i \geq 0 \text{ for } i = 0, 1, \ldots, k.$$

This represents the most important case since with the proper number of impulse functions located at the proper locations on the interval $[0, 1]$ one can model any form of the detection probability distribution. Referring back to row three in the table, the two terms in the fault coverage have an intuitive explanation. The term $(1 - \alpha_0)$ represents the highest achievable fault coverage since α_0 is the fraction of faults with zero detection probability (redundant faults). The second term is negative, hence the quantity inside the summation sign represents the fraction of undetected faults. This quantity is a sum of decaying exponentials with time constants ($ln(1 - x_i)$'s) dependent on the position of the delta functions. The saturation value of the fault coverage due to an exponential is given by the strengths (α_i's) of the corresponding delta function. If the actual $p(x)$ distribution can indeed be approximated by the small number of well-spaced delta functions, the foregoing analysis suggests a novel way of visualizing the fault coverage curve. The (exponential) rise in fault coverage in a particular part of the curve arises from a group of faults with roughly equal detection probabilities. If the groups are arranged in a decreasing order of detection probabilites, the earlier groups dominate the first part (from left to right) of the curve and the last groups are active at its tail end.

In addition, a knowledge of the $p(x)$ parameters from the initial course of test generation allows us to predict fault coverage without performing fault simulation. This result is significant since fault simulation is a major contributor to the overall test generation process [12]. For combinational circuits the costs of generating deterministic tests dominates the overall test generation process. For sequential circuits, however, the fault simulation cost often dominates. As an example, we provide the data on sequential test generation for a chip with 4856 faults. A random sample of 1000 faults was chosen for test generation. A sequence of 842 test vectors was generated and found to cover 98.2% of the faults in the sample. In another run, the fault coverage of the same sequence of test vectors was determined to be 82% over the whole fault population. The run times for this experiment on a VAX 8650 computer were as follows.

Test Generation: 64,062 sec.

Fault Simulation: (Sample) 86,585 sec.
(All faults) 462,234 sec.

5 Evaluating the $p(x)$ Parameters from Fault Coverage

We evaluate the $p(x)$ distribution according to the model presented in the previous section. Analytical solution to the problem is not possible since, in general, the fault coverage y_n has no closed form solution. In practice the fault coverage of n vectors (random or deterministic) is found by using fault simulators such as [2].

From the coverage data, one can comute the value of the unknown parameters as follows. Model $p(x)$ as

$$p(x) = \sum_{i=0}^{i=9} \alpha_i \delta(x - 0.1i),$$

where $\delta(x - x_0)$ is the Dirac delta function at $x_0, \sum_{i=0}^{i=9} \alpha_i = 1$, and $\alpha_i \geq 0$ for $i = 0, 1, \ldots, 9$. That is, $p(x)$ is modeled as a series of 10 impulse functions equally spaced on the interval [0,1] with α_0 equal to the strength of the impulse function at zero (we have chosen 10 equally spaced functions for simplicity; a general model may include more impulse functions with varying strengths at varying locations). Substituting $p(x)$ in equation (1) for random coverage we obtain:

$$\begin{aligned} y_n &= 1 - \int_0^1 (1 - x)^n \left(\sum_{i=0}^{i=9} \alpha_i \delta(x - 0.1i) \right) dx \\ &= 1 - \sum_{i=0}^{9} \int_0^1 \alpha_i (1 - x)^n \delta(x - 0.1i) dx \\ &= 1 - \sum_{i=0}^{i=9} \alpha_i (1 - 0.1i)^n \end{aligned} \qquad (1)$$

Assume that the random coverage is known for at least the first 9 vectors. Denote the known coverage in increasing order as $y_1, y_2, \ldots, y_9$

From the above we have the following system of linear equations.

$$\begin{cases} y_0 = 1 - \alpha_0 - \alpha_1 - \cdots - \alpha_9 \\ y_1 = 1 - \alpha_0 - .9\alpha_1 - \cdots - .1\alpha_9 \\ y_2 = 1 - \alpha_0 - (.9)^2\alpha_1 - \cdots - (.1)^2\alpha_9 \\ \vdots \\ y_9 = 1 - \alpha_0 - (.9)^9\alpha_i - \ldots - (.1)^9\alpha_9, \end{cases}$$

which can be written as

$$C = AX, \qquad (2)$$

where

$$\begin{aligned} c_i &= 1 - y_i, \ \ c_0 = 1, \\ x_i &= \alpha_i, \ \ and \\ a_{ij} &= (1 - 0.1j)^i, \quad i, j = 0, 1, 2, \ldots, 9. \end{aligned}$$

Equation (3) can be solved numerically by standard methods [5] to obtain the values of $\alpha_0, \alpha_1, \ldots, \alpha_9$.

6 Applications to Benchmark Circuits

We used the proposed method of computing the parameters of $p(x)$ on three of the larger ISCAS circuits [4]: C2670, C6288 and C7552. Tests were generated for each circuit using a podem [6] test generator for deterministic test generation and a deductive [2] fault simulator running on a VAX 8600 computer.

When the above method of evaluating $p(x)$ was employed, we obtained non-meaning full negative values for some of the alpha parameters. The reason for such values is easily explainable. The fault coverage data was obtained from a fault simulator on just one sample of random vectors. For a small sample of random vectors the coverage is dependent on the type of random (or deterministic) patterns chosen. Our analysis does not take this fact into consideration.

Alternatively we used the Minitab statistical package to estimate the alpha parameters. Using the Regress command on a table with row i of the form

$$\left((1 - y_i), (.9)^i, (.8)^i, \ldots, (.1)^i\right),$$

one can estimate the alpha parameters for the proposed model. An R^2 value reflecting the accuracy of the estimated parameters for the data is also given. The number of rows in the data must exceed the number of alpha parameters for the procedure to work.

We formed the proper tables for the three large ISCAS circuits and used Minitab. We formed 12 vectors for each of the C2670, C6288, and C7552 circuits, respectively.

For the C2670 circuit we obtained,

$$p(x) = 0.367 + 0.146\delta(x - 0.1) + 0.486\delta(x - 0.3),$$

with R-Square value of 99.82.

For the C6288 circuit,

$$p(x) = 0.0814 + 0.794\delta(x - 0.3) + 0.124\delta(x - 0.9),$$

with R-Square value of 99.93.

And, for the C7552 circuit, we obtained,

$$p(x) = 0.3254 + 0.665\delta(x - 0.2),$$

with R-Square value of 99.71.

The accuracy of our model is clearly reflected in the R^2 values given. Note that the $p(x)$ distribution for the C6288 circuit relative to the C2670 and C7552 is more skewed to the right. This indicates that the C6288 circuit is less resistant to random testing than either of the other two circuits. This result is well supported by what is known about these three circuits.

7 Conclusion

In this paper we have presented a new method of computing the detection probability distribution of a combinational circuit from fault coverage data. The proposed procedure is a topology independent method which differs from procedures already existing. We modeled the detection probability distribution as a series of impulse functions of varying strengths over the interval $[0,1]$. The accuracy of the model is a function of the number of impulse functions used and on the location of the impulse functions. We found that a model of 10 impulse function that are equaly distributed over the interval $[0,1)$ resulted in high R^2 values, reflecting the accuracy of the estimates. We are currently investigating the use of a beta model for the testability profile. The advantages of this model over the present model is the continuity of $p(x)$ over the interval $[0,1]$.

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