Laboratory demonstration week of: February 8, 2016

1 Introduction

For this laboratory you will design, implement, and demonstrate an 8-to-1 multiplexer and 3-to-8 decoder. These are simple combinatorial circuits.

2 Components

You can use the template at:
http://www.ittc.ku.edu/~gminden/EECS_443_Laboratory/Laboratory/EECS_443_VHDL_Header_Template.vhd
for your designs.

2.1 8-to-1 Multiplexer

Design, implement, demonstrate, and document an 8-to-1 multiplexer in VHDL. The multiplexer shall have:

1. 8 input signals from Nexys 4 switches SW<15..8>
2. 3 select signals from Nexys 4 switches SW<2..0>
3. An enable signal from switch SW<3>
4. An output signal to LED<0>

The behavior of the 8-to-1 Multiplexer shall be:

1. All signals are “High True,” that is a “True” value is represented by a ‘1’.
2. If the enable is False, i.e. ‘0’, the output of the multiplexer is ‘0’
3. Otherwise, the select signals determine which input signal is routed to the output. If the select signals are ‘000’ then the input from SW<8> is routed to the output. If the select signals are ’111’ then the input from SW<15> is routed to the output.

Implement a top-level component to demonstrate your design.

2.2 3-to-8 Decoder

Design, implement, demonstrate, and document a 3-to-8 decoder in VHDL. The decoder shall have:

1. 3 select signals from Nexys 4 switches SW<2..0>
2. An enable signal from switch SW<3>
3. 8 output signals to LED<7..0>

The behavior of the 3-to-8 Decoder shall be:
1. All signals are “High True,” that is a “True” value is represented by a ‘1’.

2. If the enable is False, i.e. ‘0’, all outputs of the multiplexer are ‘0’.

3. Otherwise, the select signals determine which input signal is True. If the select signals are ‘000’ then LED<0> shall illuminate. If the select signals are ‘111’ then LED<7> shall illuminate.

Implement a top-level component to demonstrate your design.