EECS 443 Laboratory Exercise #2

Laboratory demonstration week of: February 1, 2016

1 Introduction

For this laboratory you will design, implement, and demonstrate an Full Subtractor and Comparator. These are simple combinatorial circuits.

2 Components

You can use the template at:
http://www.ittc.ku.edu/~gminden/EECS_443_Laboratory/Laboratory/EECS_443_VHDL_Header_Template.vhd
for your designs.

2.1 Full Adder

Design, implement, demonstrate, and document an FULL ADDER in VHDL. The full adder shall have:

- 1. 3 input signals from Nexys 4 switches
- 2. 1 Difference output signal
- 3. 1 Borrow output signal

Implement a top-level component to demonstrate your design.

2.2 4 Bit Comparator

Design, implement, demonstrate, and document a 4 BIT COMPARATOR in VHDL. The COMPARATOR shall have:

- 1. 2 input signals 4 bit each from Nexys 4 switches
- 2. 3 output signals to LED indicating greater, equal and less than.

Implement a top-level component to demonstrate your design.