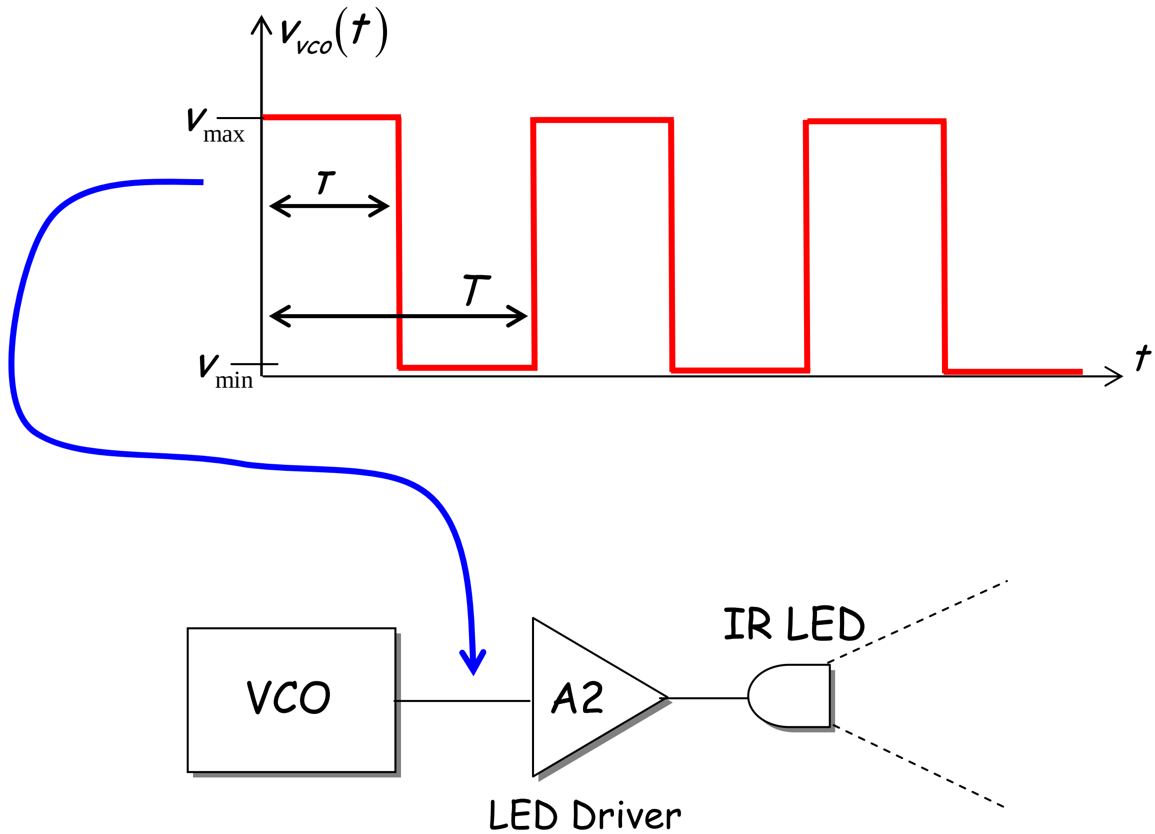
Driving your LED's

As we have previously learned, in optical communication circuits, a **digital signal** with a frequency in the tens or hundreds of **kHz** is used to **amplitude modulate** (on and off) the emissions of a Light Emitting Diode (LED):



The question then is: how do we use this square wave to "**turn on**" and "**turn off**" the LED?

First, we must use the **precise language** and nomenclature of electronic devices. An LED—as its name makes clear—is a **diode**.

However, most LED are not silicon junction diodes but instead are made of **Gallium Arsenide** (GaAs). This makes them somewhat different than the p-n junction diodes we studied in EECS 312, but the **basics** are the same.

1. An LED **emits** IR energy (it is "on") when the diode is **forward biased**. For silicon p-n junction diodes, significant but plausible (i.e., non-destructive) forward bias current results in a forward bias diode voltage drop (from anode to cathode) of between 0.5 and 0.9 volts. Thus, we typically **approximate** this forward biased voltage as 0.7 V.

However, for GaAs LEDs this forward bias voltage is between **1.0 and 2.0** volts when the diode current is significant (i.e., > 1 mA) yet plausible (i.e., < 1 A).

2. An LED does **not** emit IR energy (it is "off") when the diode is **reverse biased**. In this state, the diode current is essentially **zero**. There is of course a transition region between the forward and reverse bias states (i.e., their definitions are a bit **subjective**), but we can safely say that an LED is reverse biased ($i_D = 0$) when its diode voltage is less than (say) 0.5 V.

Q: *So, just how do we take the output of the VCO and use it to place the diode in one of these two state?*

A: The answer is the LED **driver**.

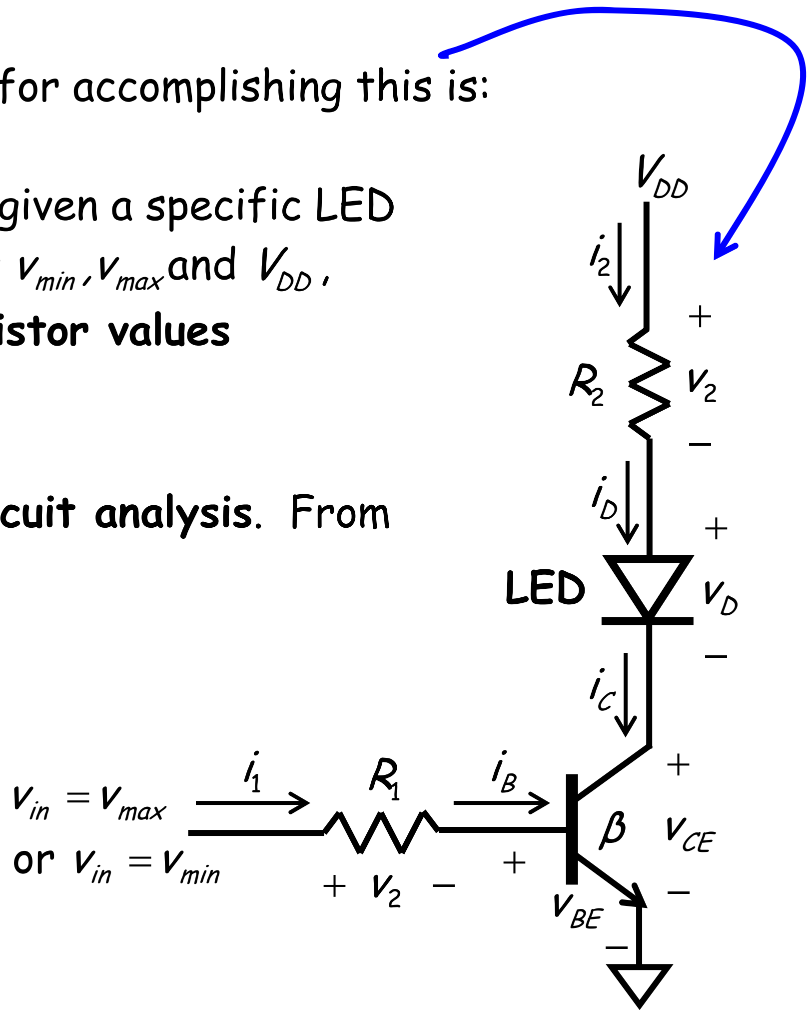
As we look at the "digital" signal from the VCO, we see it has one of **two** voltage states—either high voltage v_{max} or low voltage v_{min}. Our job is to "map" each of these two voltage states into a diode bias state of either reverse or forward.

An **excellent** driver circuit for accomplishing this is:

The design problem is this: given a specific LED and BJT, as well as voltages v_{min}, v_{max} and V_{DD}, what should be the **two resistor values** R_1 and R_2?

To begin, let's do a little **circuit analysis**. From KCL:

$$i_2 = i_D = i_C \quad \text{and} \quad i_1 = i_B$$



From KVL:

$$V_{DD} - v_2 - v_D - v_{CE} = 0 \quad \text{and} \quad v_{in} - v_1 - v_{BE} = 0$$

And finally from Ohm's Law:

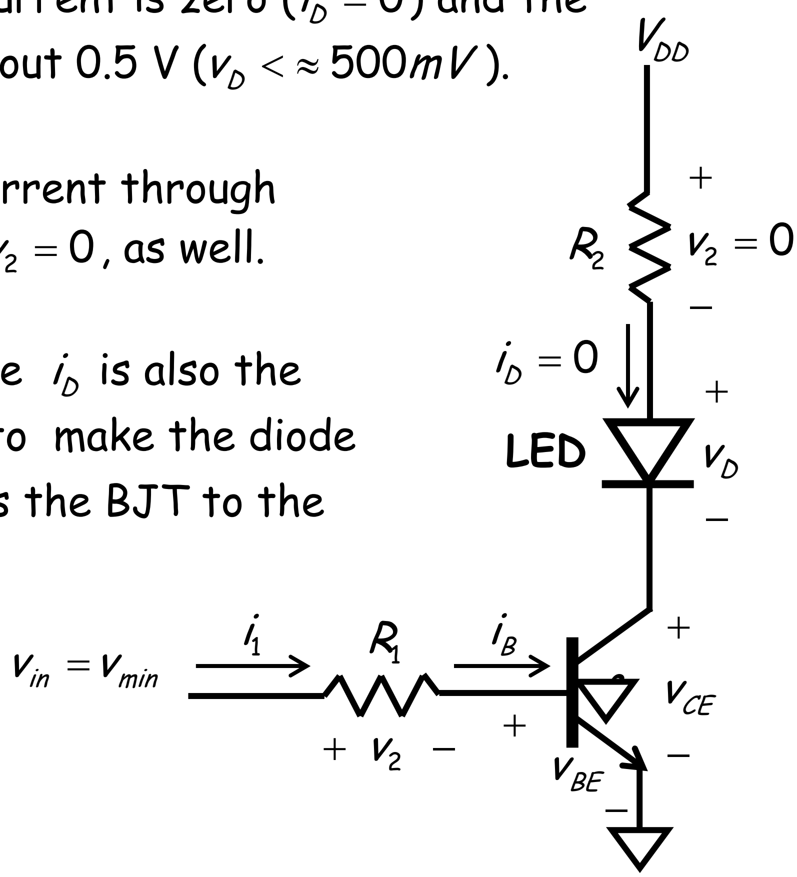
$$i_1 = \frac{v_1}{R_1} \qquad \text{and} \qquad i_2 = \frac{v_2}{R_2}$$

Now, it is reasonable to decide that when $v_{in} = v_{min}$ the LED should be **reverse** biased (off) and when $v_{in} = v_{max}$, the LED should be **forward** biased (on).

Let's look at the **reverse bias case first**. We know that for this to be true, the diode current is zero ($i_D = 0$) and the diode voltage is less than about 0.5 V ($v_D < \approx 500 mV$).

Note this means that the current through resistor R_2 is **zero**, so that $v_2 = 0$, as well.

But, by KCL we know that the i_D is also the collector current i_C. Thus, to make the diode reverse biased, we must bias the BJT to the proper **mode**.



Q: *I see! We must make the npn BJT either "on" or "off", right?*

A: NO!!!!!! Transistor modes are **not** "on" or "off". There are three—count em'—**three** specific and unambiguous transistor modes. For Bipolar Junction Transistor (BJT), these modes are **Active, Saturation, and Cutoff**.

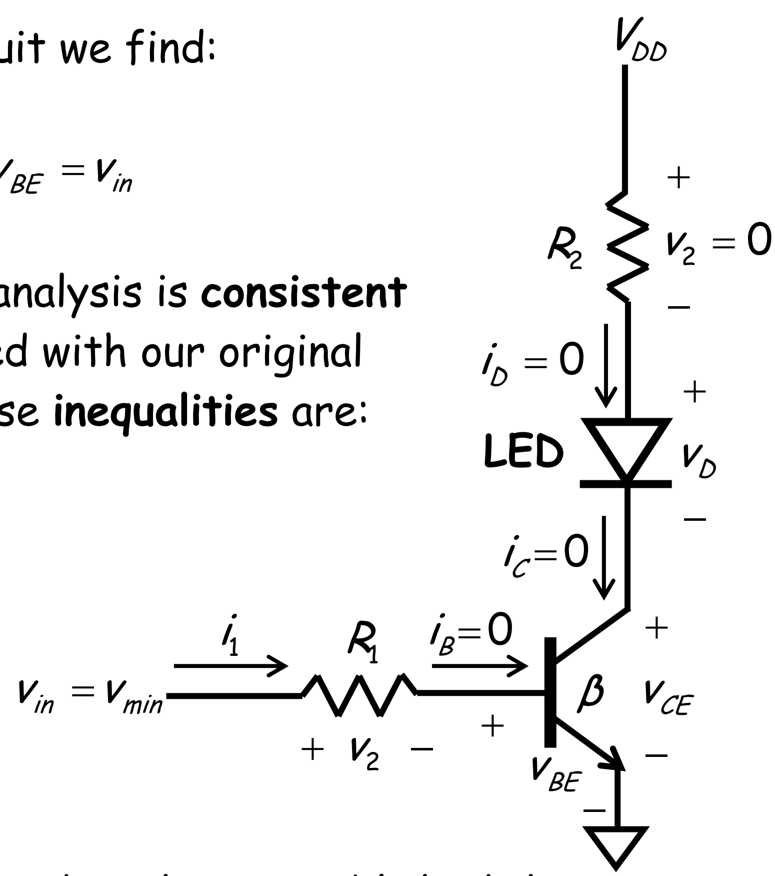
Hopefully, the correct mode for the reverse biased transistor is **evident**. We require that $i_D = i_C = 0$, and all transistor currents are zero if the BJT is in **cutoff**!

→ If the BJT of our circuit is in **cutoff** mode, the LED will be **reverse** biased.

So, let's ASSUME that our BJT is in **cutoff**. Recall that we ENFORCE the equalities $i_B = i_C = i_E = 0$.

If we now ANALYZE this circuit we find:

$$v_D = V_{DD} - v_{CE} \qquad \text{and} \qquad v_{BE} = v_{in}$$



We now CHECK to see if this analysis is **consistent** with the **inequalities** associated with our original cutoff assumption. Recall these **inequalities** are:

$$v_{CE} > 0.7\,V \qquad \text{and} \qquad v_{BE} < 0$$

Now **if** the LED is reverse biased, we have established that $v_D < 0.5\,V$, meaning that for this circuit assumption

$$v_D = V_{DD} - v_{CE} < 0.5 \qquad \Rightarrow \qquad v_{CE} > V_{DD} - 0.5$$

Thus, in order for $v_{CE} > 0.7V$, the voltage source V_{DD} **must** be:

$$V_{DD} - 0.5 > 0.7 \qquad \Rightarrow \qquad V_{DD} > 1.2V$$

This means that V_{DD} **must** be greater than 1.2 V for the BJT to be in **cutoff**. This of course is not much of a restriction, as V_{DD} is **always** much greater than 1.2 volts!

From the second inequality, we can conclude that in order for the BJT to be in cutoff, the input voltage v_{min} must be **negative** (i.e., $v_{min} < 0$) !

Q: *Yikes! I'm **not sure** that this will be the case. Although v_{min} will likely be **zero** (or at least very small), I don't think it will actually be **negative**!?!*

A: Well, the inequality $v_{BE} < 0$ is actually a little bit **too restrictive**. Remember, the important thing here is that the Base-Emitter Junction (BEJ) of the BJT is **reverse biased**. Again, this definition is a little **nebulous**.

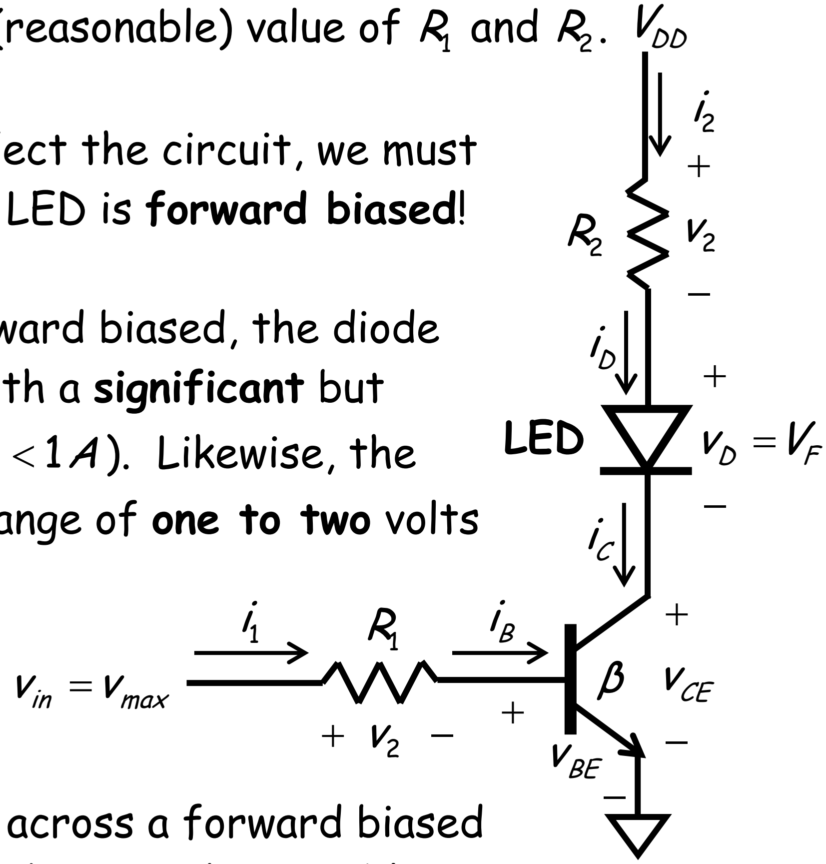
Clearly, the BEJ will be reverse biased if $v_{BE} < 0$, but it likewise will exhibit **almost no diffusion current** if v_{BE} is **positive but small**. A less restrictive, but **nearly** as accurate inequality would be $v_{BE} < 0.3V$. Meaning that $v_{min} < 0.3V$ is required for the BJT to be in cutoff. This restriction is quite **realistic**.

Thus we can conclude for our driver circuit, the LED will be reverse biased (off) if **both** these conditions are satisfied:

$$V_{DD} > 1.2V \quad \text{and} \quad v_{in} = v_{min} < 0.3V$$

Q: *Hey wait a minute! **Neither** of these design statements have anything to do with **resistors** R_1 and R_2. Where do **they** come in??*

A: If the BJT is in **cutoff**, they don't! If the two inequalities above are satisfied, then the BJT will be in cutoff and the LED reverse biased for **any** (reasonable) value of R_1 and R_2.



To see how the resistors affect the circuit, we must consider the case where the LED is **forward biased**!

Recall that if the LED is forward biased, the diode current i_D will be **positive**, with a **significant** but plausible value (e.g., $1\,mA < i_D < 1\,A$). Likewise, the diode voltage will be in the range of **one to two** volts (i.e., $1V < v_D < 2V$).

LED vendors call the voltage across a forward biased LED the "forward voltage" and give it the variable V_F.

Since now we have a case where $i_C = i_D > 0$, the BJT is clearly **not** in cutoff. Of course it could be in either **1) saturation** or **2) active mode**. Let's see if we can design a driver for **each** mode!

First, we must determine what diode current we **desire** when the LED is forward biased (vendors typically refer to this as **forward current** I_F). Of course, the higher the current, the "brighter" our LED light. From that standpoint, we wish to make that current as **large as possible**.

Q: *Can we just make it **really** large—like, say, **10 Amps**?*

A: Unfortunately **no**.

We attempted to put that much current through an LED, we would surely **melt** it.

Every diode has a **maximum power rating** P_D^{max}. The power absorbed by the diode is simply the product of the voltage across and the current through it. Of course, these values will be **changing with time** as $v_{vco}(t)$ toggles between v_{max} and v_{min}.

The **time-averaged** power dissipation, however, can be determined and—**not** surprisingly—it depends on the **duty cycle** τ/T of signal $v_{vco}(t)$:

$$P_D = I_F V_F \left(\frac{\tau}{T}\right)$$

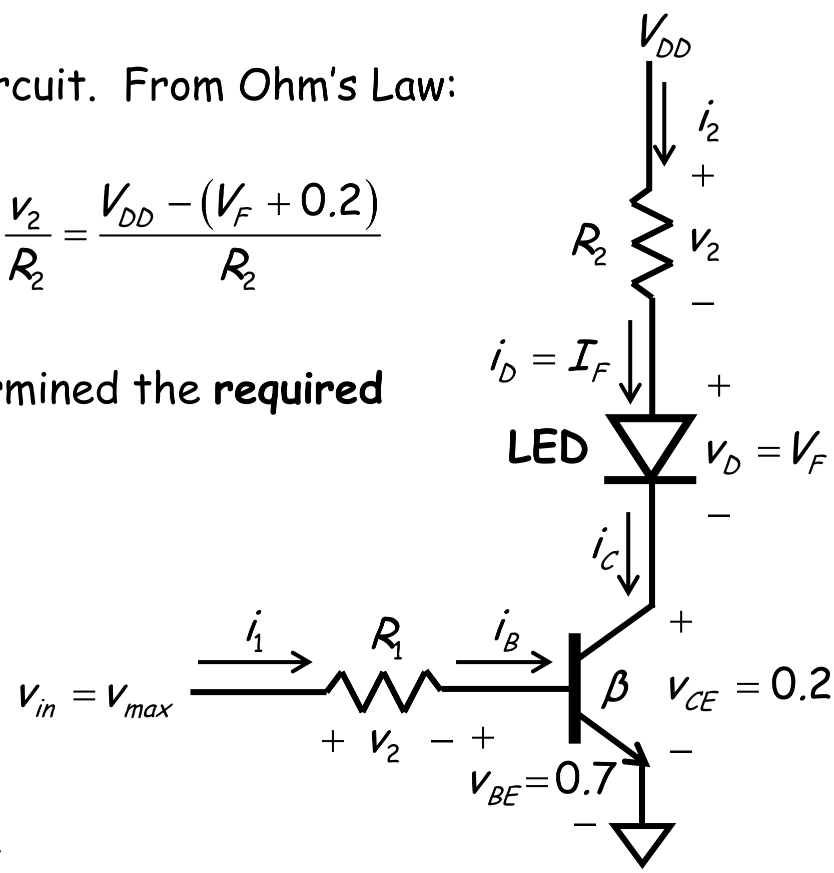
Since we wish to **avoid melting**, we want $P_D^{max} > P_D$ meaning:

$$I_F V_F \left(\frac{\tau}{T}\right) < P_D^{max} \qquad \Rightarrow \qquad I_F < \frac{P_D^{max}}{V_F}\frac{T}{\tau}$$

Once we have **selected a suitable** I_F we can design the LED driver. Let's **first** ASSUME that the BJT is in **saturation**. We ENFORCE equalities:

$$v_{BE} = 0.7\,V \quad \text{and} \quad v_{CE} = 0.2\,V$$

Now we ANALYZE this circuit. From Ohm's Law:



$$I_F = i_2 = \frac{v_2}{R_2} = \frac{V_{DD} - (V_F + 0.2)}{R_2}$$

Rearranging, we can determined the **required** value of resistor R_2:

$$R_2 = \frac{V_{DD} - (V_F + 0.2)}{I_F}$$

Likewise:

$$i_B = i_1 = \frac{v_1}{R_1} = \frac{v_{max} - 0.7}{R_1}$$

Now we must CHECK our results to see if/when they are **consistent with the inequalities** associated with BJT **saturation**. Specifically, the inequality $i_C < \beta\, i_B$.

Since $i_C = I_F$, this inequality leads to:

$$I_F < \beta\left(\frac{v_{max} - 0.7}{R_1}\right) \qquad \Rightarrow \qquad R_1 < \beta\left(\frac{v_{max} - 0.7}{I_F}\right)$$

Thus, we conclude that the BJT **will** be in saturation, with collector current $i_C = I_F$, **if**:

$$R_2 = \frac{V_{DD} - (V_F + 0.2)}{I_F} \qquad \text{and} \qquad R_1 < \beta\left(\frac{v_{max} - 0.7}{I_F}\right)$$

The problem with this design **could** be the resulting base current:

$$i_B = \frac{v_{max} - 0.7}{R_1}$$

It is possible that the VCO **cannot provide that much current**. Thus, an alternative design can features the BJT in **active** mode.

For this mode, we ENFORCE the equalities:

$$v_{BE} = 0.7\ V \qquad \text{and} \qquad i_C = \beta\, i_B$$

And so now ANALYZE this circuit:

$$i_B \beta = i_C = I_F \qquad \Rightarrow \qquad i_B = \frac{I_F}{\beta}$$

and as before:

$$i_B = i_1 = \frac{v_1}{R_1} = \frac{v_{max} - 0.7}{R_1}$$

combining:

$$\frac{I_F}{\beta} = \frac{v_{max} - 0.7}{R_1} \qquad \Rightarrow \qquad R_1 = \beta \frac{v_{max} - 0.7}{I_F}$$

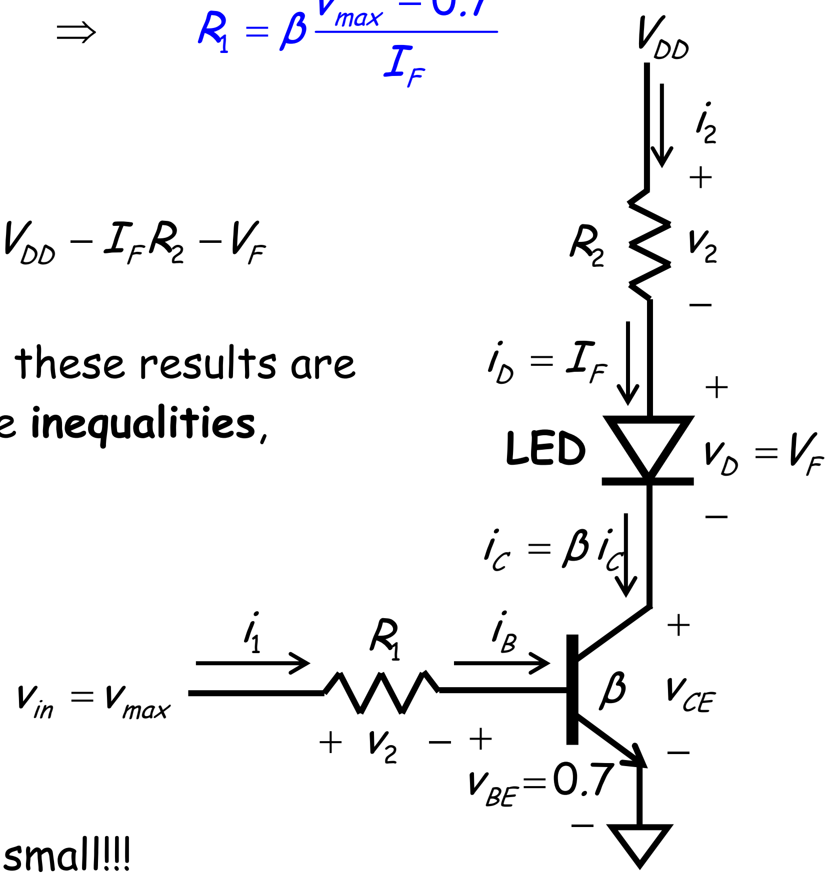
Likewise:

$$v_{CE} = V_{DD} - I_F R_2 - V_F$$

Now CHECK to see if/when these results are **consistent** with active mode **inequalities**, specifically $v_{CE} > 0.7$.

$$v_{CE} = V_{DD} - I_F R_2 - V_F > 0.7$$

$$\Rightarrow \qquad R_2 < \frac{V_{DD} - V_F - 0.7}{I_F}$$



Caution: don't make R_2 too small!!!

Thus, the BJT **will** be in active mode, and the LED current **will** be I_F, **if**:

$$R_1 = \beta \frac{v_{max} - 0.7}{I_F} \qquad \text{and} \qquad R_2 < \frac{V_{DD} - V_F - 0.7}{I_F}$$